CDT TECH DAY

JUNE 11TH 2024

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CDT Tech Day, June 11th 2024

AI-Infused Electronic Systems Design

Delivering new levels of productivity and capability

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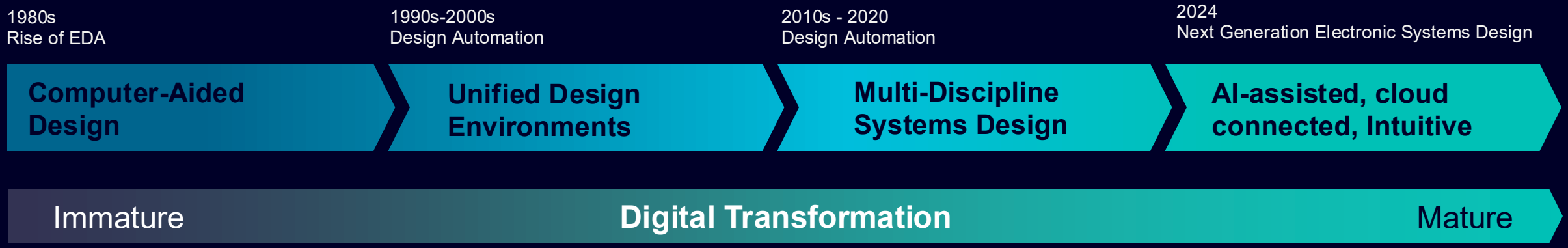
Evolution of Electronic Systems Design



A roadmap to innovate faster and accelerate the delivery of your advanced electronic products

Overcome resource constraints and addressing competitive pressures

Develop resilience and adaptability to chronic unpredictability

Accelerate digital transformation initiatives and AI/ML implementation

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Siemens and AI

Just a few examples of at-scale use of Siemens AI today outside of EDA

Mobility

Schedule & route planning, predictive management

Energy

Optimization of gas and wind turbine installations

Industrial

Automated visual inspection, factory optimization

Medical

Predictive maintenance, diagnostic assistance

Siemens has been **deploying AI, at-scale,** across diverse industries **delivering significant quality of life improvements** to people all over the globe.

https://www.siemens.com/global/en/company/innovation/research-development/ai-lab.html

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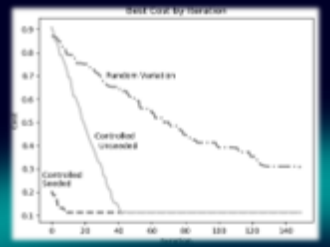
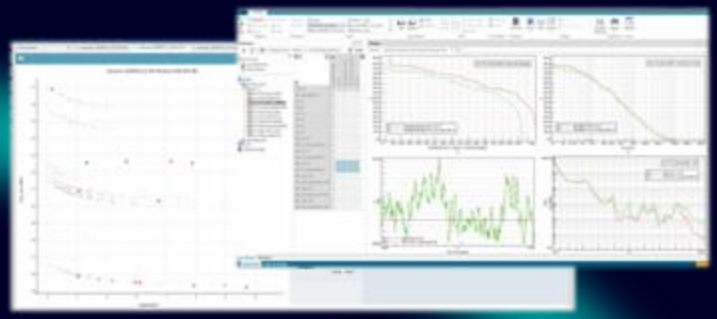
Siemens AI expertise delivered for design….

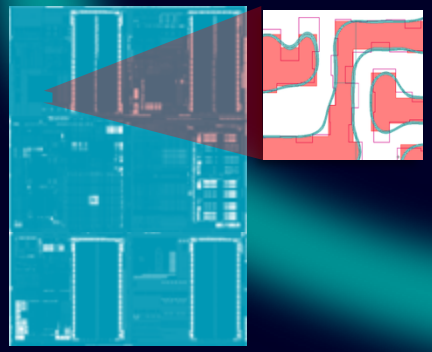
NX adaptive user interface



HyperLynx
Design space exploration &
PDN optimization

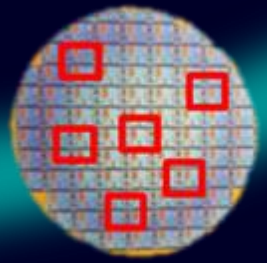


Simcenter design decision support, model-based system testing & smart controls

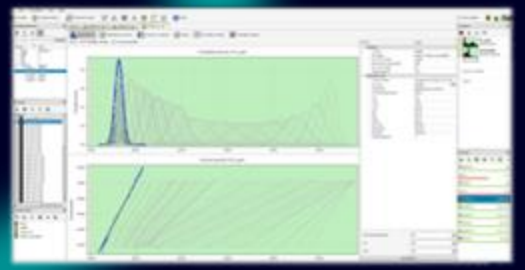


Calibre OPC & LFD
IC verification

Supplyframe supply
chain analysis



Tessent yield analysis



Solido variation designer

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Removes the barriers of complexity, accelerates productivity, and delivers positive experiences for engineers and their teams

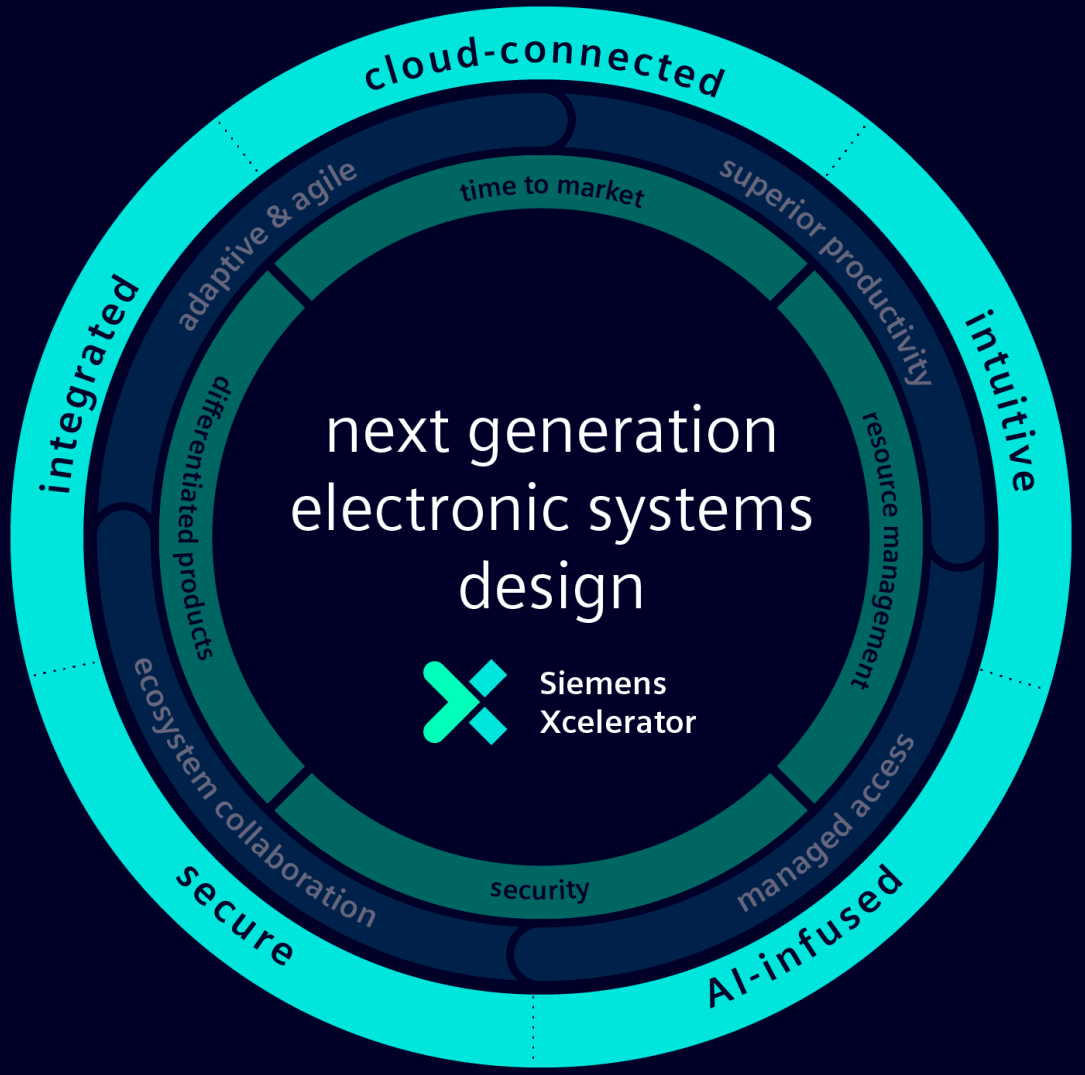
Intuitive
Boost productivity with a modern user experience

AI-infused
Accelerate design optimization and automation

Cloud-connected
Collaborate seamlessly across the ecosystem

Integrated
Leverage digital threads across multiple domains

Secure
Ensure the protection of critical design IP



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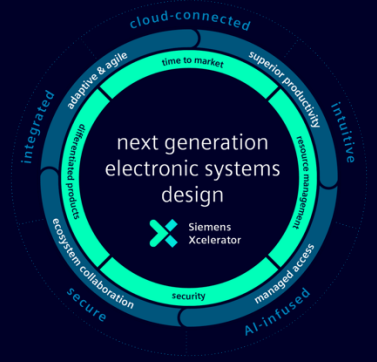


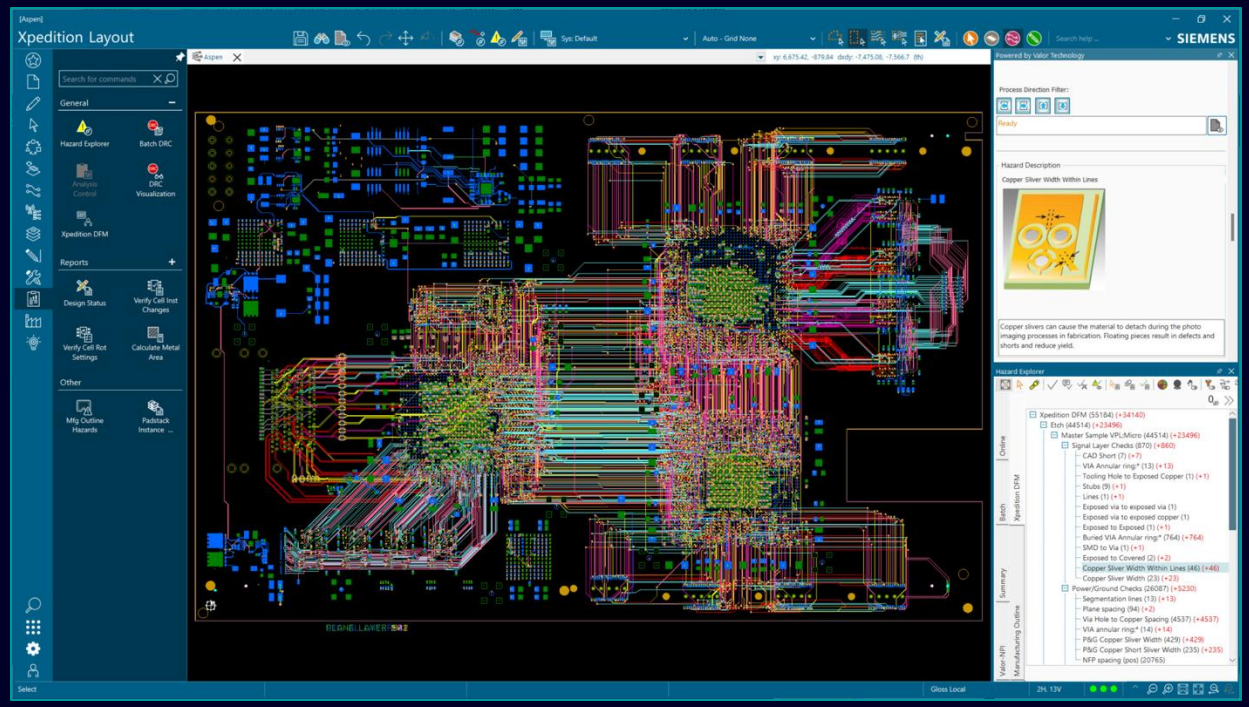
Intuitive

Removes the barriers of complexity

- Superior user & team productivity
- Lowered learning curve
- Results in positive experiences

> “Was able to figure things out before reading instructions”

> “Just looking at it makes you want to use the tool more”



Select Beta Customer Quotes

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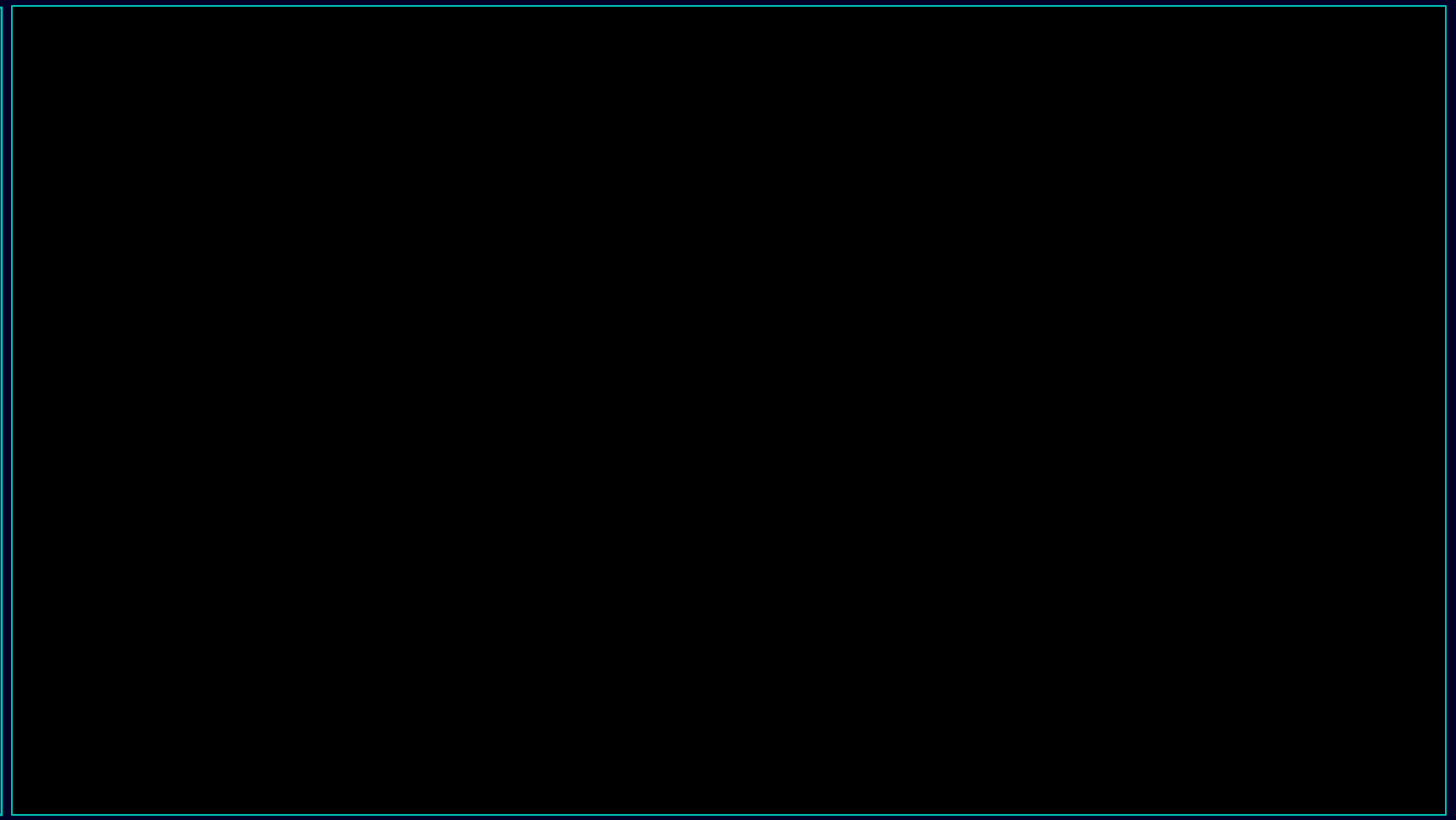
UX Overview

Intuitive

Removes the barriers of complexity



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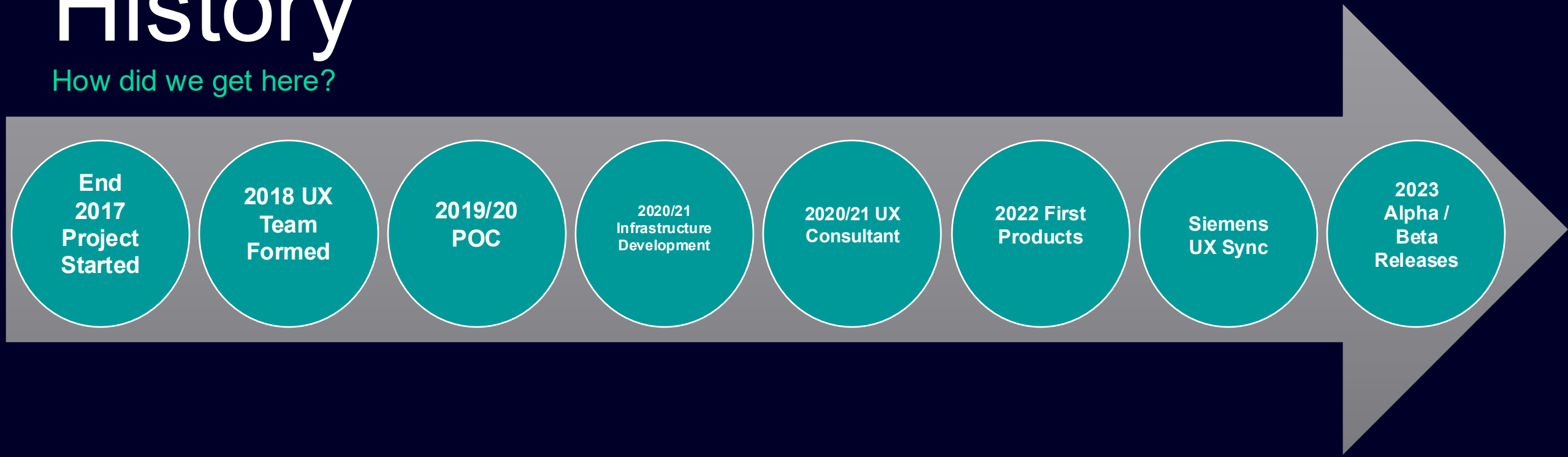
Next-Generation UX History

How did we get here?



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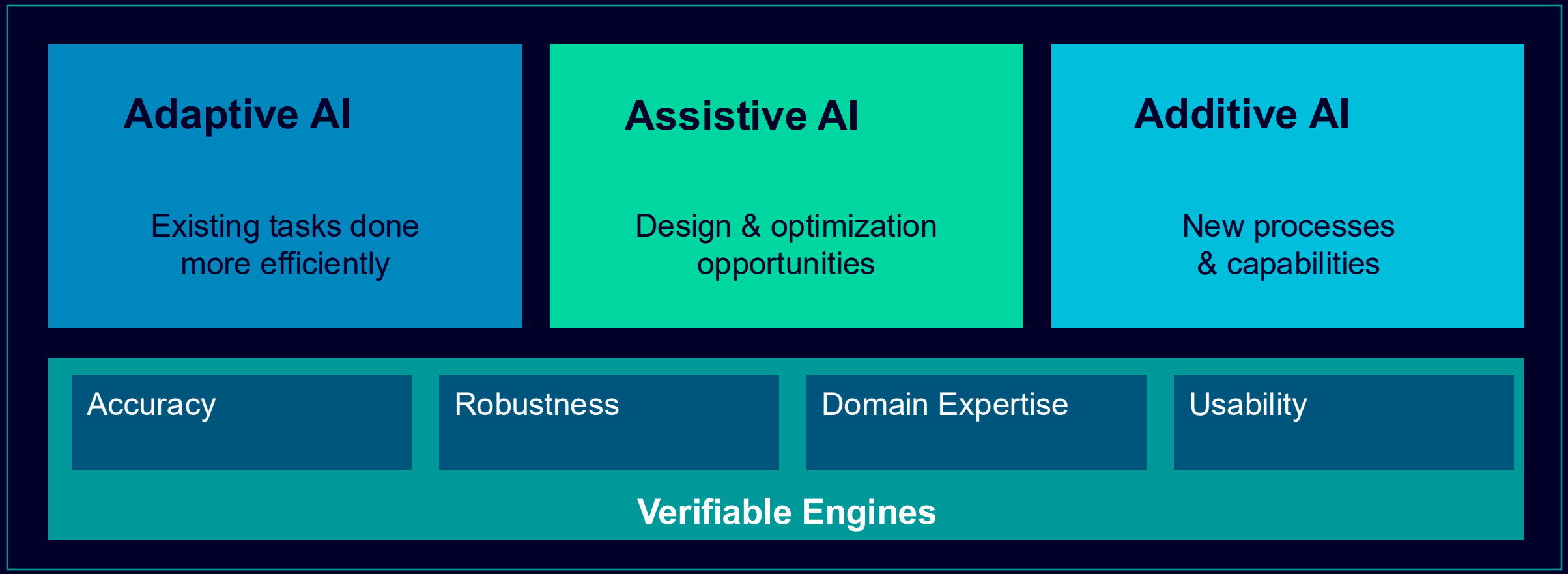
AI solutions built with verifiability at their core



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Enabling AI-driven electronic systems design

Evolution of capability

Adaptive AI

Existing tasks done more efficiently

Accelerate in-tool decision making to increase designer productivity.

Leveraging design data and best practices to enable personalized experience and smart human interaction

Targeted use cases:

- Process/command prediction
- Product support
- Component recommendation
- Supply chain prediction
- Constraint prediction
- Net unravelling

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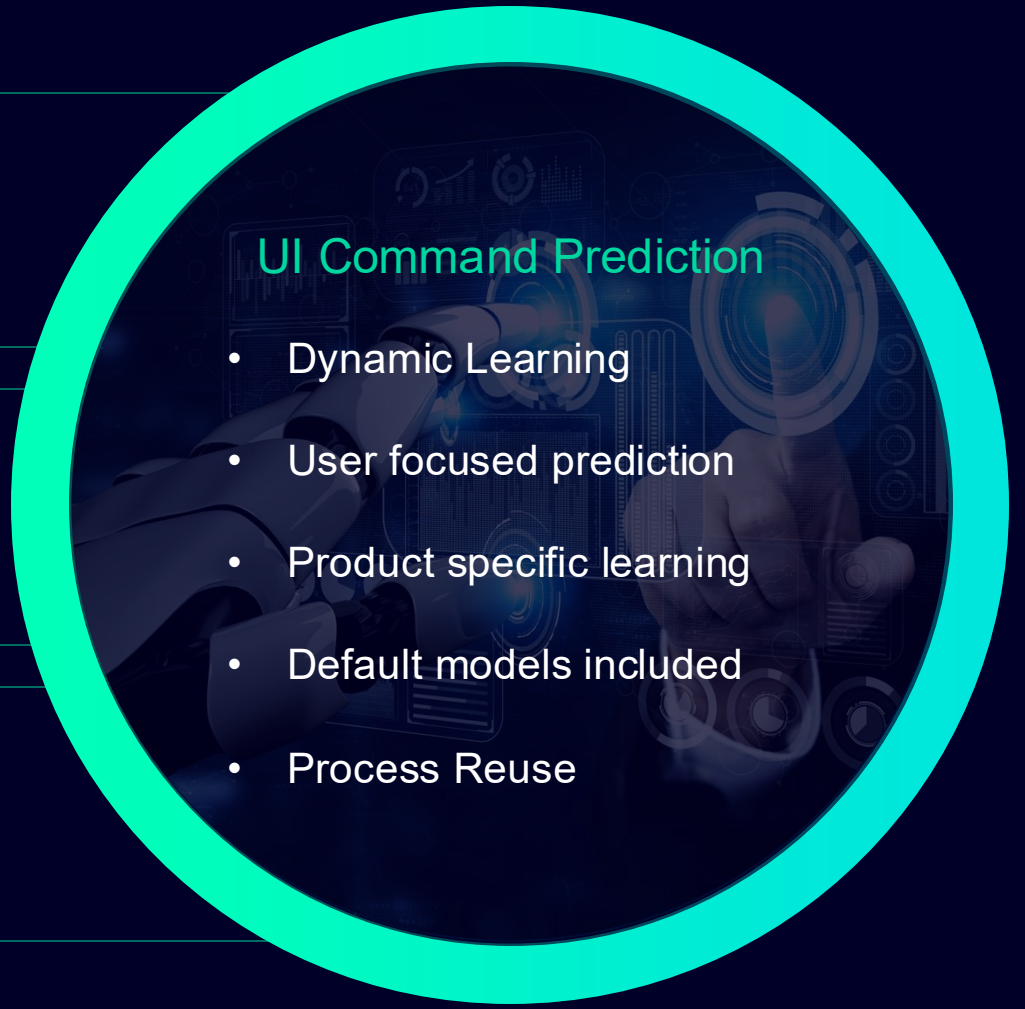
Foundation of Predictive Engineering
AI and ML for Electronic Systems Design

Utilize extracted information from completed designs to train AI/ML models

Develop prediction systems, based on trained models

Enhance existing solutions to incorporate prediction systems to make recommendations



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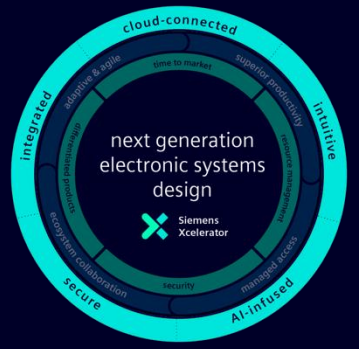


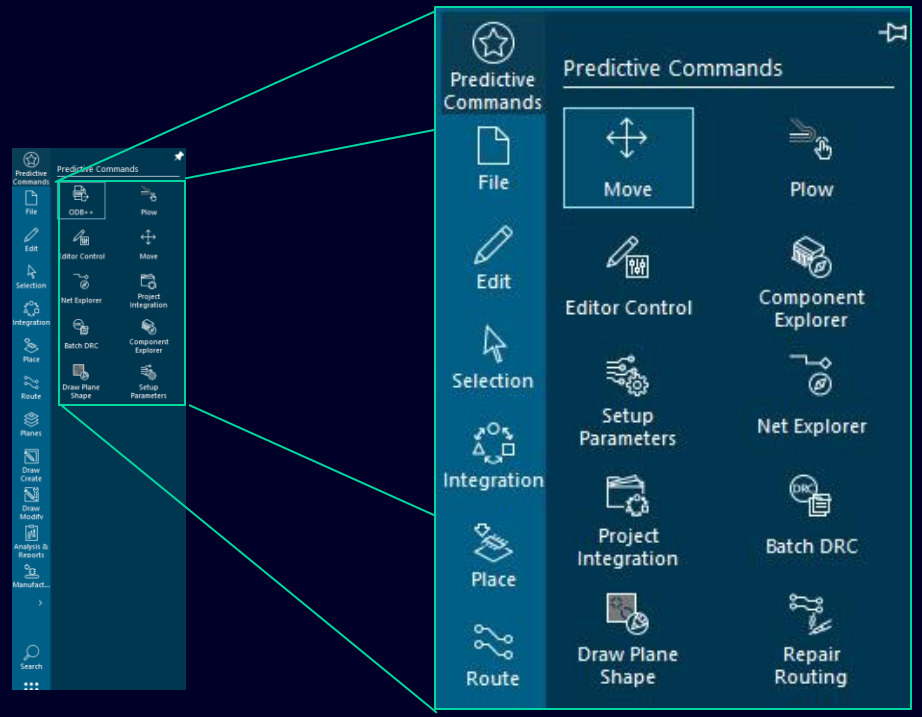
AI-infused

Expands engineering capacity without additional resources

> “This is the best prediction engine I've seen in EDA software so far. ”

Select Beta Customer Quotes

- Data collection and preprocessing
- Model training
- Inference & prediction
- Feedback loop



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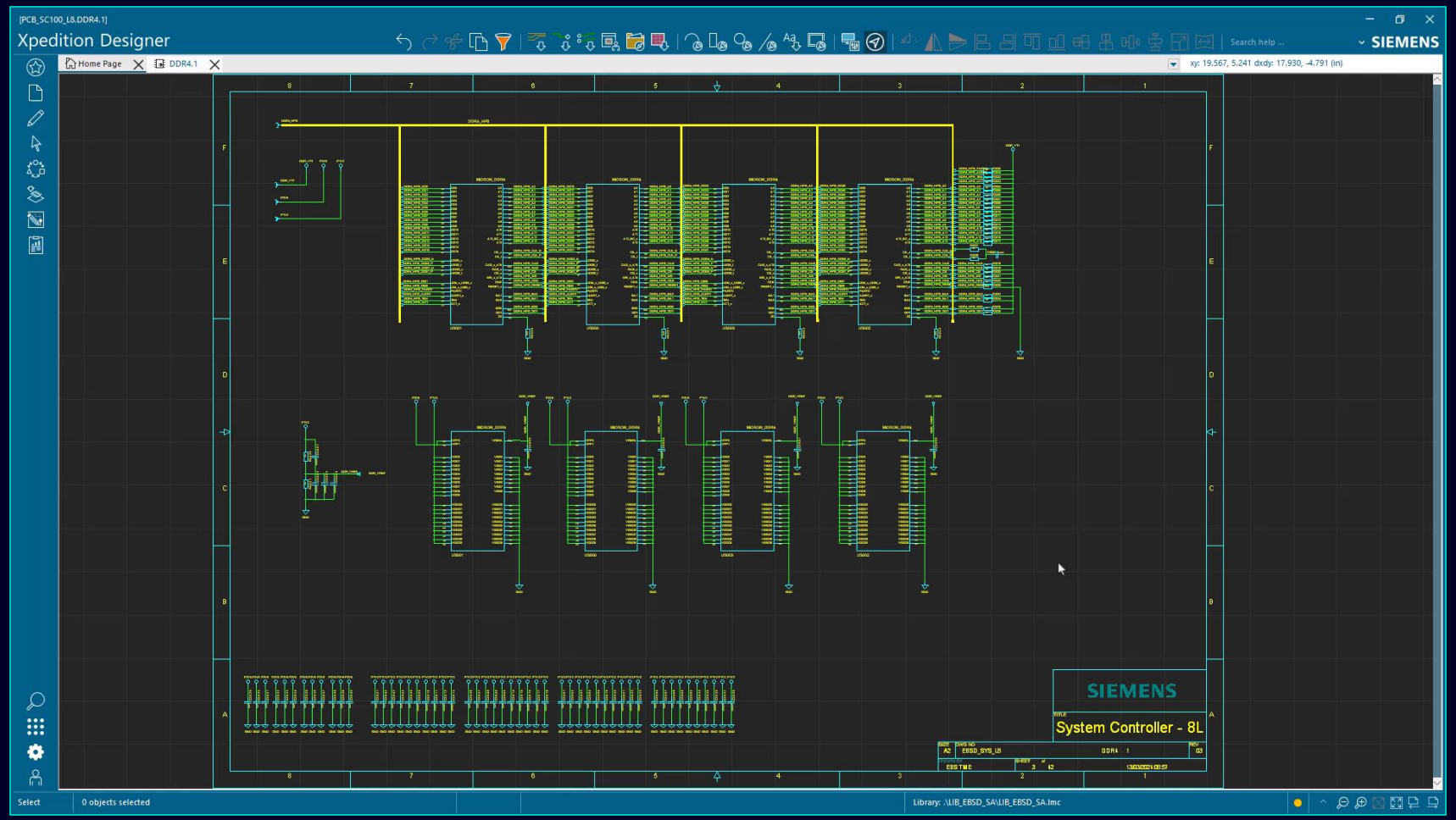
Predictive Commands

AI-infused

Accelerate design optimization and automation



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Process Prediction Models

Process Prediction models are stored on each user's system and are specific to the product and user. We expect customers to want to back up these models and possibly share them among users.

- The ML Models are located at: C:\Users\<user>\AppData\Roaming\Siemens\EBS\XENTP2409\ML
- Filenames are hardcoded to each product
- These files cannot be shared between products by renaming them, i.e. use Layout model with Fablink

Value : Encourages best practices

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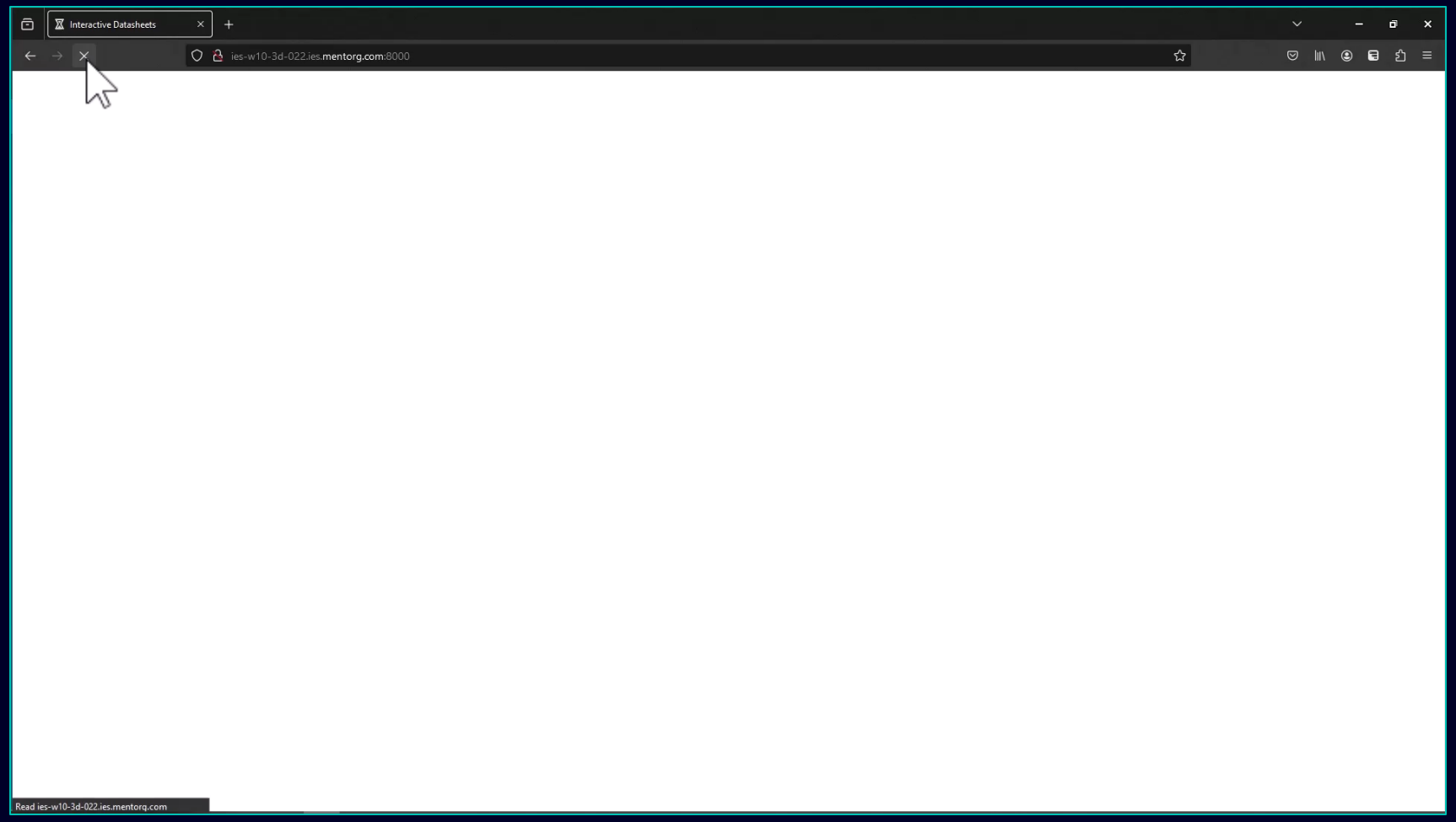
Interactive Datasheets

AI-infused

Accelerate design optimization and automation



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Enabling AI-driven electronic systems design

Evolution of capability

Assistive AI

Design & optimization opportunities

Optimize designs by exploring solution space and making recommendations.

Design space exploration and surrogate modeling to enable optimization, enhanced simulation, and comprehensive analysis across the electronic system

Targeted use cases:

- Decoupling capacitors
- Via transitions
- BGA breakouts
- Channel analysis
- Advanced simulation

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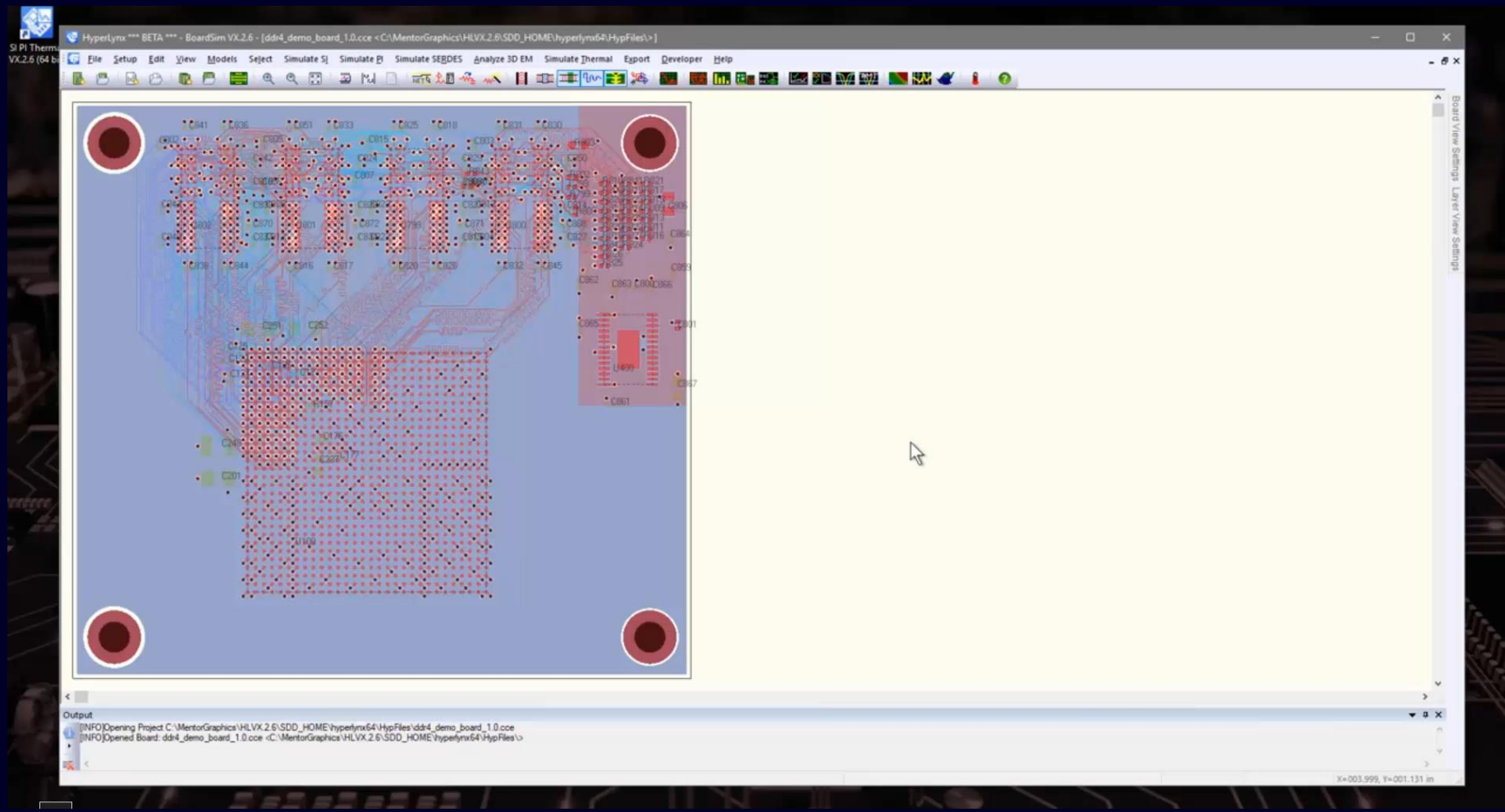
Decoupling capacitors optimization
Example

Load the layout into HyperLynx boardsim

Setup the extraction and default models

Extract the mode for the layout and launch the PDN capacitor optimizer

View the report



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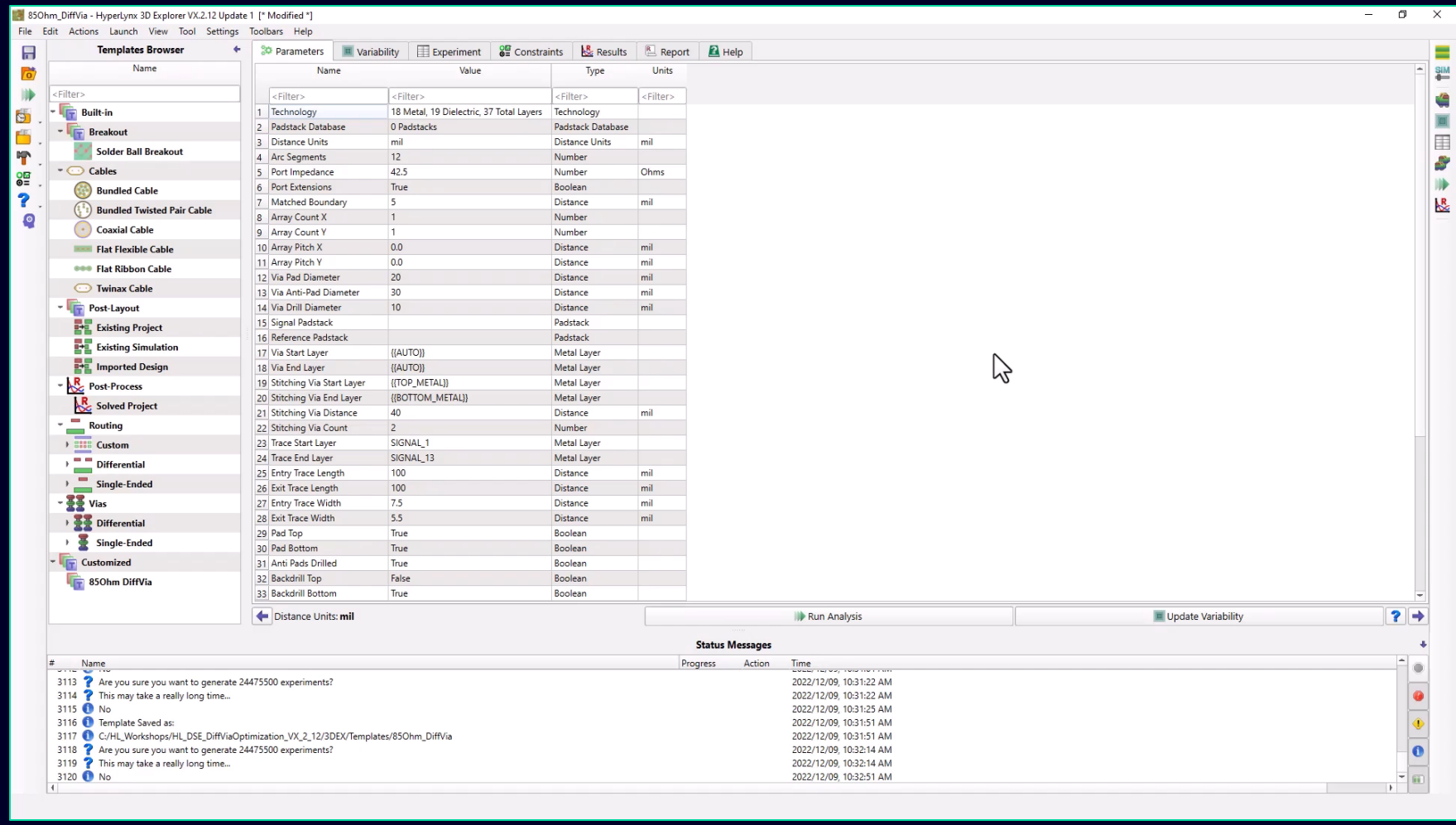
Design Space Exploration
Example

Define available CPUs & target # evaluations

Define design variables & optimization goals

Engine optimally explores space & recommends best option

Create surrogate models to accelerate future analyses



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Enabling AI-driven electronic systems design

Evolution of capability

Additive AI

New processes & capabilities

Accelerate design process through automation.

Reinforced learning models to direct deep learning and/or intelligence delivered through large language models to enable subject matter expertise at the point of design

Targeted use cases:

- Schematic connectivity
- Library model creation
- Advanced auto-routing
- Component placement
- Generative design

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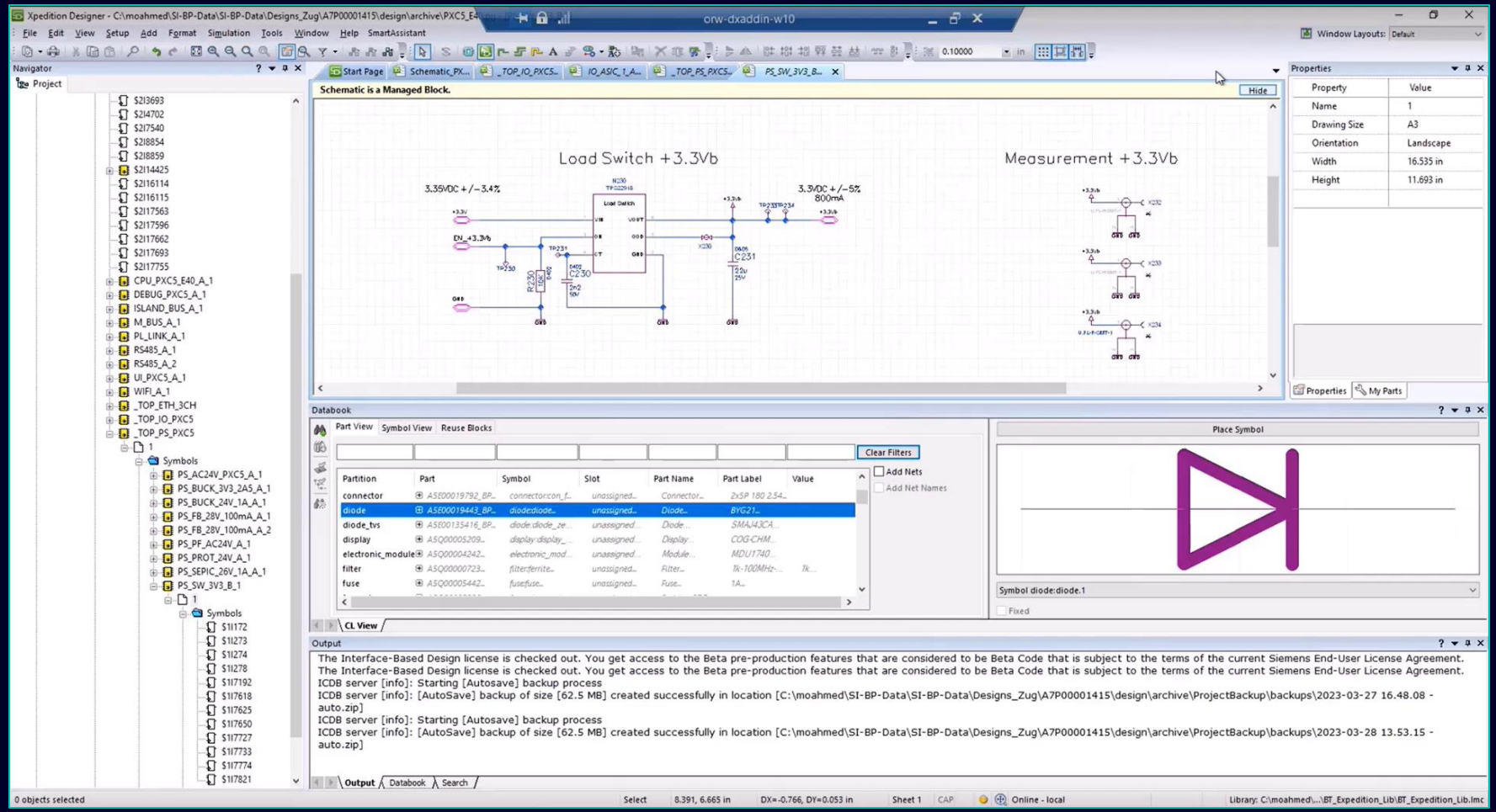
Component Recommend

AI-infused

Accelerate design optimization and automation



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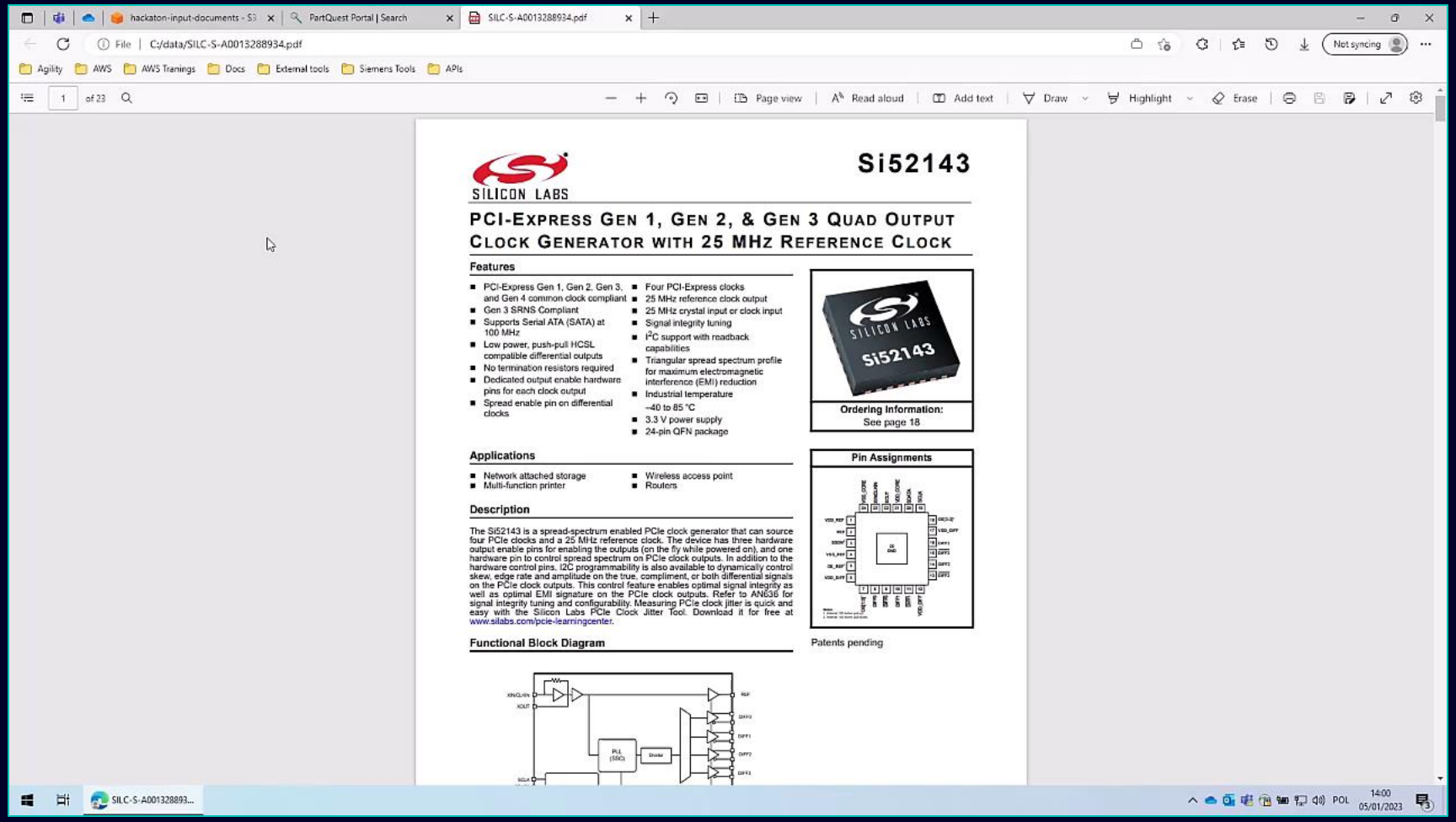
Datasheet Extraction

Symbol Generation

AI-infused

Accelerate design optimization and automation



Si52143

SILICON LABS

PCI-EXPRESS GEN 1, GEN 2, & GEN 3 QUAD OUTPUT CLOCK GENERATOR WITH 25 MHZ REFERENCE CLOCK

Features

- PCI-Express Gen 1, Gen 2, Gen 3, and Gen 4 common clock compliant
- Gen 3 SRNS Compliant
- Supports Serial ATA (SATA) at 100 MHz
- Low power, push-pull HCSL compatible differential outputs
- No termination resistors required
- Dedicated output enable hardware pins for each clock output
- Spread enable pin on differential clocks
- Four PCI-Express clocks
- 25 MHz reference clock output
- 25 MHz crystal input or clock input
- Signal integrity tuning
- I²C support with readback capabilities
- Triangular spread spectrum profile for maximum electromagnetic interference (EMI) reduction
- Industrial temperature –40 to 85 °C
- 3.3 V power supply
- 24-pin QFN package

Ordering Information: See page 18

Pin Assignments

Applications

- Network attached storage
- Multi-function printer
- Wireless access point
- Routers

Description

The Si52143 is a spread-spectrum enabled PCIe clock generator that can source four PCIe clocks and a 25 MHz reference clock. The device has three hardware output enable pins for enabling the outputs (on the fly while powered on), and one hardware pin to control spread spectrum on PCIe clock outputs. In addition to the hardware control pins, I2C programmability is also available to dynamically control skew, edge rate and amplitude on the true, compliment, or both differential signals on the PCIe clock outputs. This control feature enables optimal signal integrity as well as optimal EMI signature on the PCIe clock outputs. Refer to AN636 for signal integrity tuning and configurability. Measuring PCIe clock jitter is quick and easy with the Silicon Labs PCIe Clock Jitter Tool. Download it for free at www.silabs.com/pcie-learningcenter.

Patents pending

Functional Block Diagram

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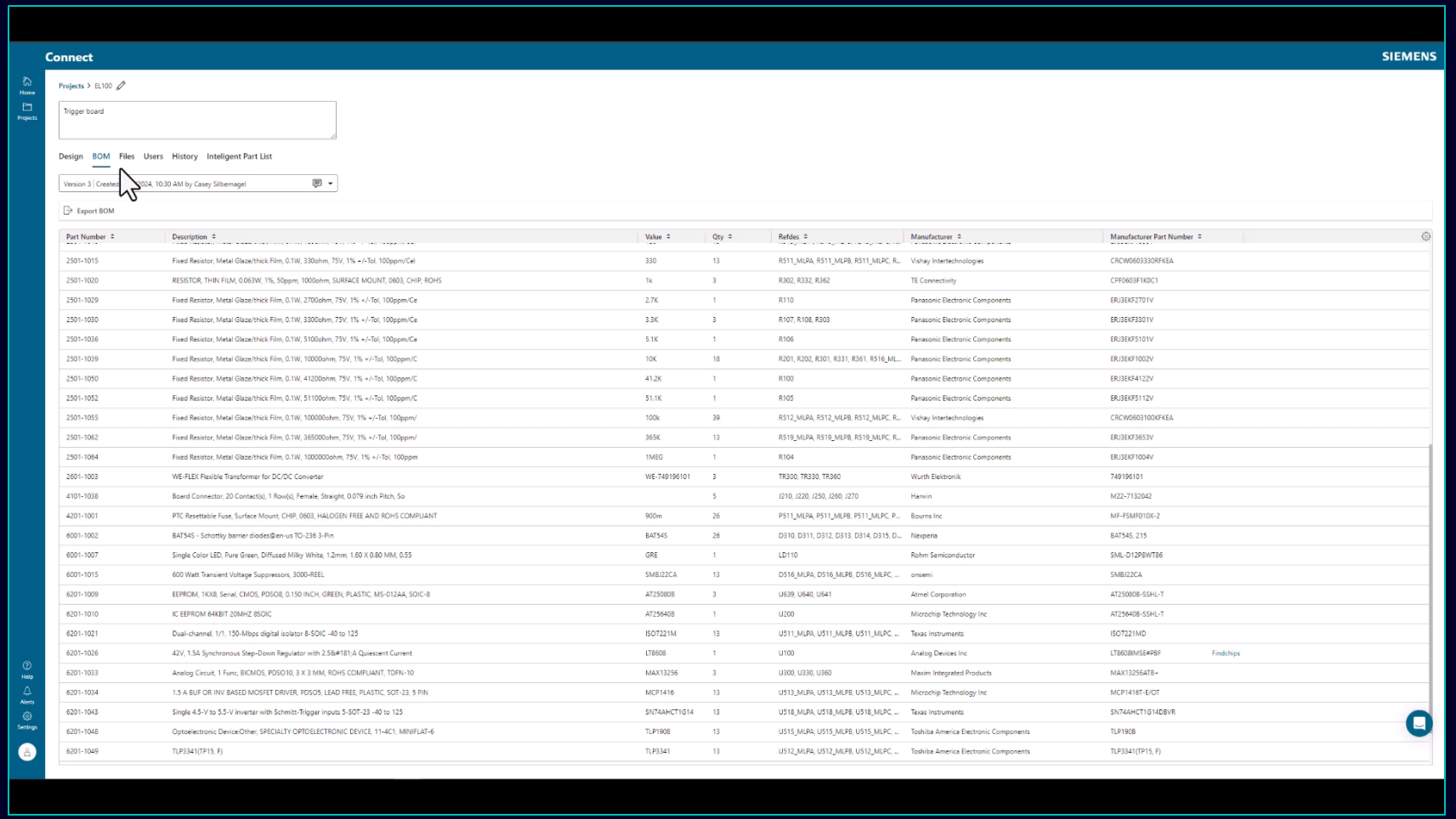
Intelligent Parts List

Cloud-connected

Collaborate seamlessly across the ecosystem



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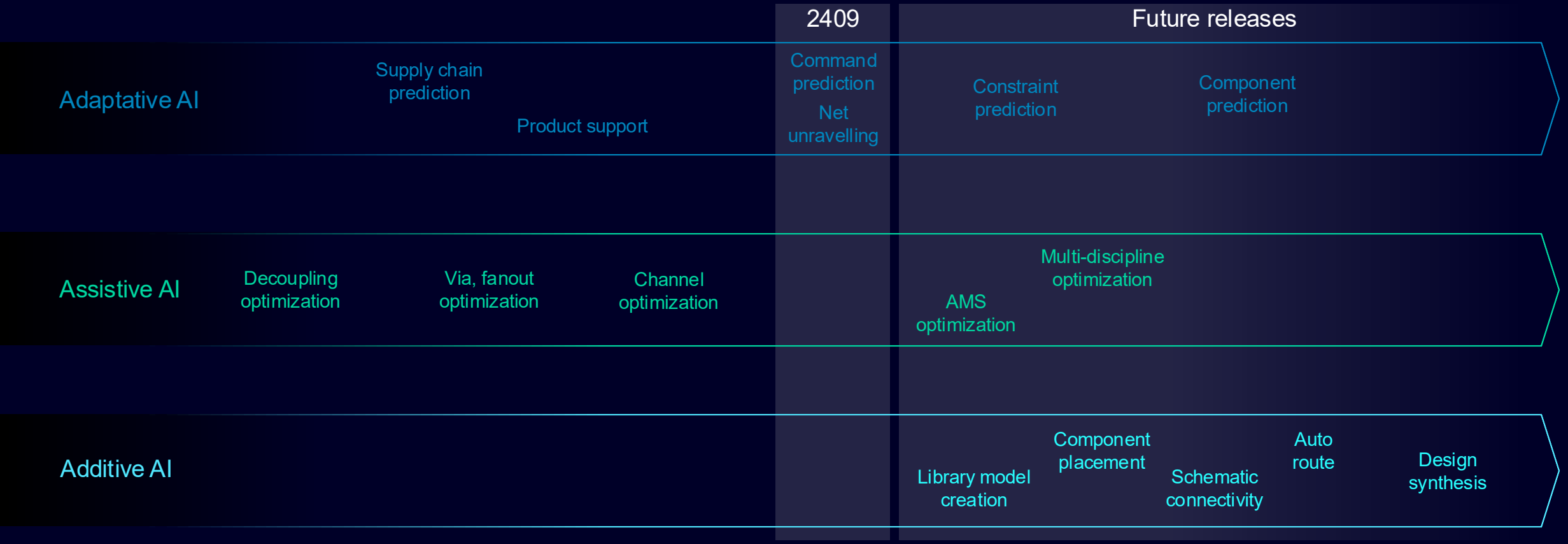
Enabling Technologies for Electronic Systems Design

Anticipated Delivery



** Timing subject to change without notice*

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Teşekkür ederim !

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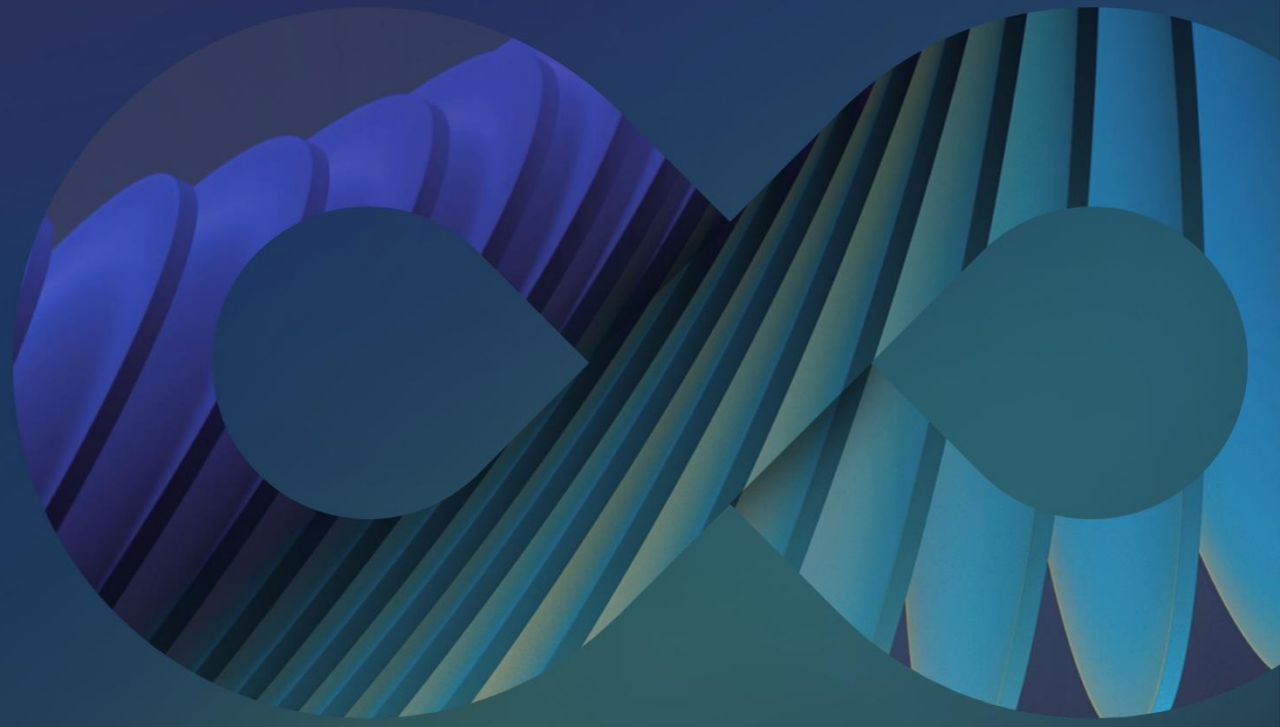
CDT Tech Day, June 11th 2024

Valydate



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AGENDA

- Product overview
- Evaluation feedback
- Conclusions
- Q&A

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Product overview

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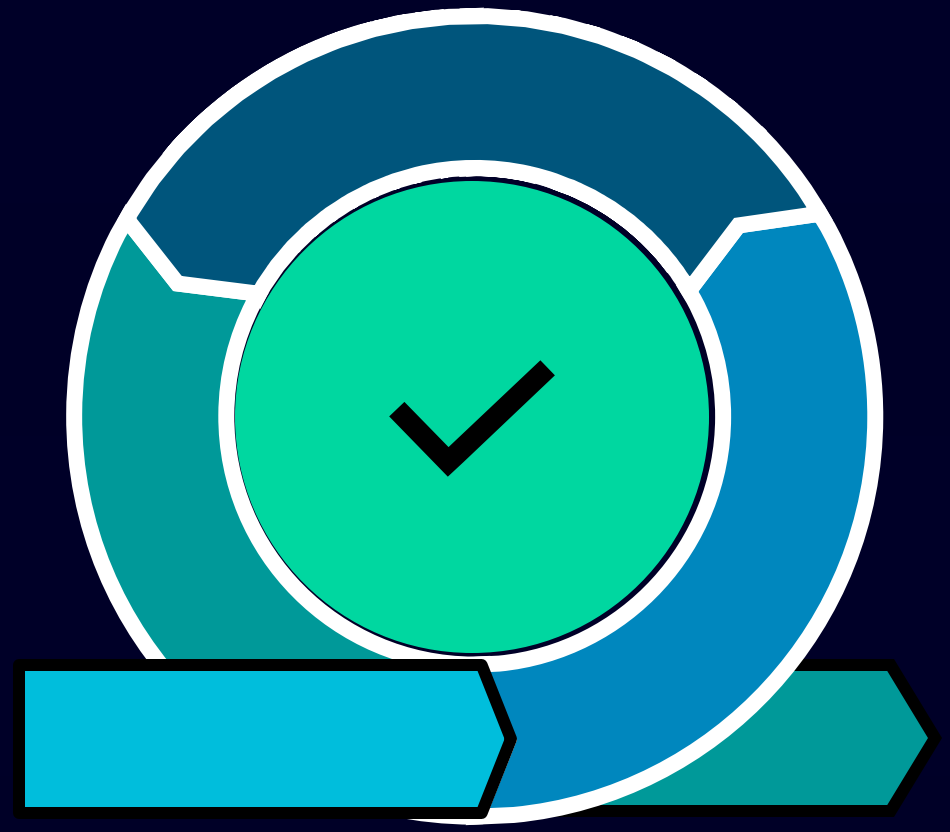
What is Valydate?

Automated parametric schematic integrity tool

1. Exhaustive, rapid, power and technology aware test of all nets in the schematic
2. Designed to reduce visual schematic inspection
3. Catches most parametric errors
4. Identifies poor design practice
5. Eliminates 50% to 70% of design re-spins caused by schematic errors and marginalities
6. Saves hardware engineers hundreds of hours of visual inspection and lab debug time



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Valydate vs. DRC

Analysis Capabilities	Valydate	DRC
Analysis using parametric model	✓	✗
Analysis using symbol	✗	✓
Single net analysis	✓	✓
Analysis through extended nets *Hierarchy, gates, filters, multiple boards…*	✓	✓
Basic IO Pin Connectivity checks *Inputs only on net, single-ended to differential…*	✓	✓
Extended Pin Connectivity checks *Polarity Swap, Mismatch Bus significance, Multiple pullups…*	✓	✗
Logic Threshold & Voltage checks *Logic-level compatibility, Pk2Pk differential signaling*	✓	✗
Pin Treatment checks *pullup/down required*	✓	✗

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Key Features

- 150+ built-in automated checks
- 10 million+ intelligent models included
- Fully inspects 100% of a schematic's nets
- Can create custom device models
- Multi-board interconnect analysis
- Easy setup and intuitive operation
- Intelligent post-processing results and reporting for tracking and audits
- Works with all major EDA tools
- Integrated setup with PADS Pro & Xpedition Designer
- No additional infrastructure required

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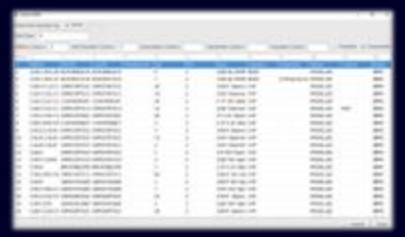
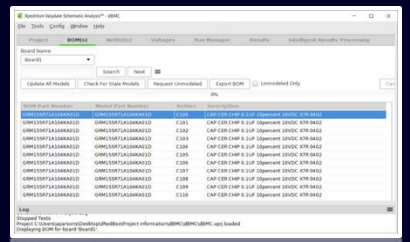
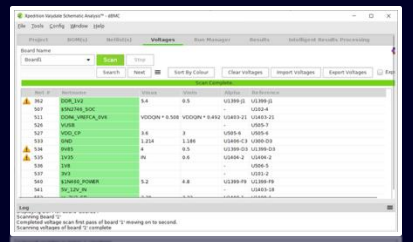
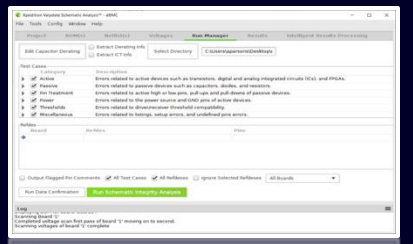
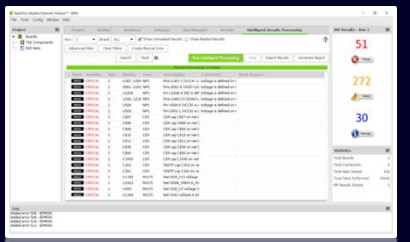
Run Valydate in 6 Easy Steps





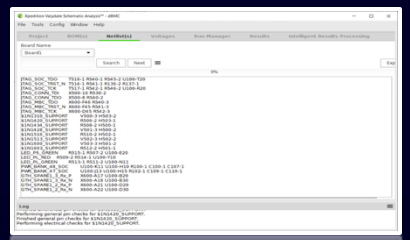






Import BOM → Assign Models → Define Voltages → Run Analysis → Review Results

Import Netlist → Define Voltages



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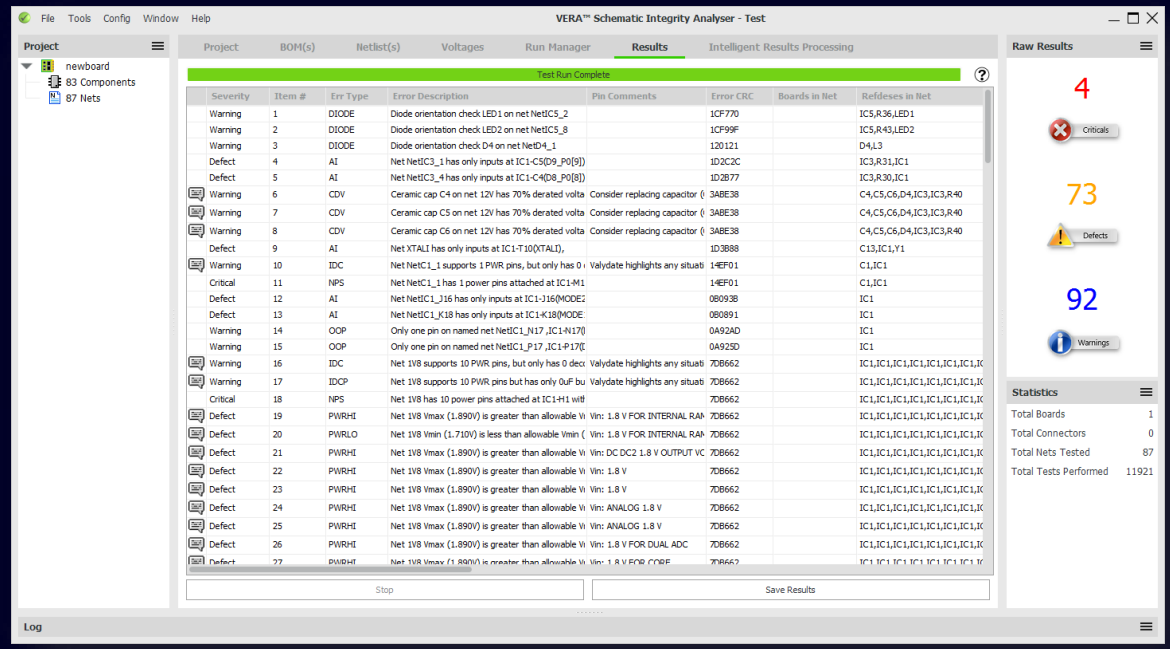
Common Issues Found

- Components not properly connected to power / ground
- Missing power source
- Capacitor decoupling sufficiency checks
- Missing pin treatments
  - *Bias resistors, timing capacitors*
- Nets missing receiver / receiver missing driver
- Incompatible pin voltage thresholds
- Wrong board-to-board connections
- Pins left floating



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Case study – average findings in 100 customer designs

Defects found

Average Metric	#
Total findings/project	84
Critical Defects/project	**5**
Defects/project	35
Warnings/project	44

Avg. Board Complexity	3218 Nets
Avg. Devices per Board	3848 Devices

High ROI

Direct savings per project (engineering and materials)	**$51,169**
Re-spins saved	**69/100**
Time to market reduction	**18 Days**

	Net	Device	Valydate Findings			Re-spin Savings		Total
Project	Count	Count	Warning	Defect	Critical	Material	Engineering	Savings
1	1220	1263	53	30	34	$36,000	$ 31,460	$ 67,460
2	1015	1165	50	18	1	$ -	$ 16,300	$ 16,300
3	1206	1408	58	7	2	$ -	$ 14,833	$ 14,833
4	1197	1477	72	1	7	$18,000	$ 17,480	$ 35,480
5	2434	5556	40	38	18	$90,000	$ 26,053	$ 116,053
6	829	1141	32	17	2	$ -	$ 12,593	$ 12,593
7	2499	2740	14	12	3	$ -	$ 7,633	$ 7,633
8	2099	2080	26	60	6	$36,000	$ 26,133	$ 62,133
9	3026	3354	118	18	6	$30,000	$ 31,987	$ 61,987
10	4006	4802	41	41	1	$60,000	$ 21,647	$ 81,647
11	1600	1686	93	57	2	$36,000	$ 37,733	$ 73,733
12	3792	4124	69	6	1	$ -	$ 16,467	$ 16,467
13	3182	3425	50	18	5	$ -	$ 17,607	$ 17,607
14	3026	3354	118	18	6	$30,000	$ 31,987	$ 61,987
15	989	1147	30	18	5	$ -	$ 13,473	$ 13,473
16	5538	5487	117	187	28	$90,000	$ 91,920	$ 181,920
17	1066	1117	37	6	0	$ -	$ 9,527	$ 9,527
18	890	1220	23	23	0	$18,000	$ 11,960	$ 29,960
19	4090	3326	11	53	8	$60,000	$ 21,493	$ 81,493
20	2804	3963	4	145	15	$60,000	$ 51,160	$ 111,160
21	2678	1996	73	70	40	$36,000	$ 50,087	$ 86,087
22	4035	4280	75	56	82	$60,000	$ 59,833	$ 119,833
23	6432	5046	43	51	3	$90,000	$ 25,847	$ 115,847
24	1024	1378	42	7	0	$ -	$ 10,873	$ 10,873
25	2101	2794	24	44	14	$36,000	$ 23,320	$ 59,320
26	2773	2849	43	2	6	$18,000	$ 11,473	$ 29,473
27	801	827	63	31	9	$ 6,000	$ 25,673	$ 31,673
28	1367	1450	75	11	1	$ -	$ 19,273	$ 19,273
29	1603	1818	37	11	1	$ -	$ 11,420	$ 11,420
30	2500	2700	16	16	12	$36,000	$ 12,240	$ 48,240
31	289	333	6	0	0	$ -	$ 1,240	$ 1,240
32	2411	3378	5	31	18	$60,000	$ 16,627	$ 76,627
33	3420	8138	101	93	3	$90,000	$ 50,993	$ 140,993
34	4252	5507	18	70	3	$90,000	$ 26,633	$ 116,633
35	740	644	77	0	7	$ 3,000	$ 18,200	$ 21,200
36	1474	1530	3	5	0	$ -	$ 2,187	$ 2,187
37	4430	4367	33	3	7	$30,000	$ 10,047	$ 40,047
38	1787	1892	12	32	1	$18,000	$ 12,833	$ 30,833
39	1500	1500	41	464	62	$36,000	$ 174,113	$ 210,113
40	444	690	0	86	3	$ 6,000	$ 27,927	$ 33,927
41	4486	4360	22	21	70	$60,000	$ 33,993	$ 93,993
42	4293	6796	3	2	1	$ -	$ 1,573	$ 1,573
								$ 82,620
								$ 5,893
								$ 143,073
								$ 52,680
								$ 78,813
								$ 48,707
								$ 4,253
								$ 41,027
								$56,638

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ROI after few designs - examples

Number of Designs / Year	Number of boards where Xpedition Valydate saves a re-spin	Total $ Savings (Engineering & Materials)
10	7	$ 358,183
20	14	$ 716,366
30	21	$ 1,074,549
40	28	$ 1,432,732
50	35	$ 1,790,915
200	140	$ 7,163,660

- Assumption: 30 new boards developed annually
- Xpedition Valydate schematic analysis will likely identify major errors on 21 out of the 30 boards
  - Total engineering and materials savings combined for all 30 designs is estimated to be over $1.0M
  - Each design would also benefit from an 18 day time to market reduction *NOT ACCOUNTED FOR IN THE ABOVE CALCULATIONS*

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Heads-up on potential development areas

- Ease model creation
  - Introduce wizards, FPGA auto-modeler, AI-based automatic model creation
- Improve analysis & handling of analog circuitry
  - MOSFET, BJT & XFMR, Opamp & Diode
- Provide users with key quality metrics
  - Setup & results metrics
- Better integrate with our products
  - EDM: Model management, invocation, results management…
  - Designer: access the results within the schematic editor…
- …and more…

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Evaluation feedback

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Customer’s Profile

- *CUSTOMER* is an international group made of 30 companies in 17 countries
- Headquarters in France
- Organized in 4 divisions: mobility, aerospace, energy, engineering services
- x6 R&D centers – 1600 persons
- x5 electronics board manufacturing plants

- The evaluation was carried out for the Automotive department

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Evaluation context

- The customer delivers a test case and expects to see what comes out in order to determine the relevance of such a product before moving forward
- A first board could not be checked because of two NXP ICs under NDA
  - Despite huge efforts I could not get their datasheets
- CPDC board selected
  - Cadence Netlist: pstxnet.dat
  - BOM: CPDC.xls
  - (optional but useful) schematics: CPDC.pdf
- Board complexity
  - 668 components (105 different references)
  - 375 nets

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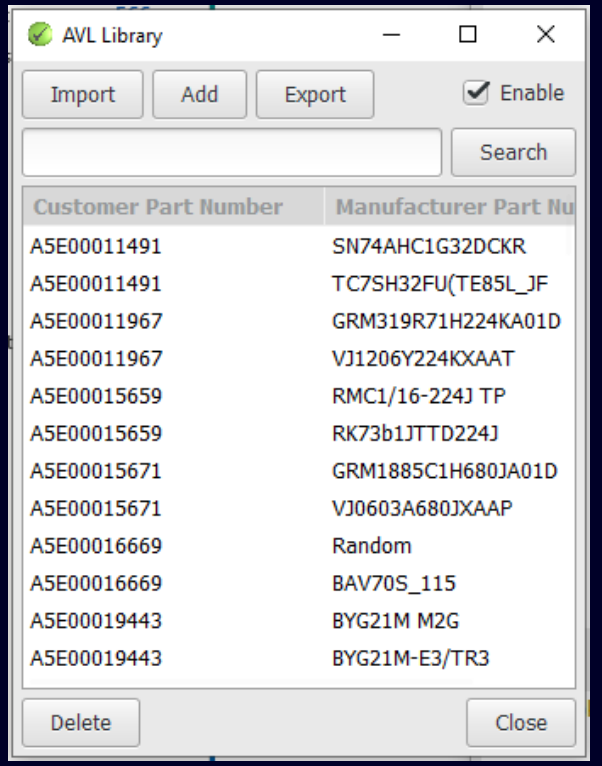
Model availability (1)

- Took a couple of days (estimated – maybe less) to gather all models
- 2 mechanical references depopulated
- Automatic model assignment:
  - 27 missing models out of 103 (105-2) references (~22%)
  - Possibility to improve the score by using “alternates” you can define in an Approved Vendor List (AVL) – not used here
- Remaining models quickly available
  - Modify existing similar models



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Model availability (2)

- FTT_Valydate can help get more models through the community
- Siemens EDA Model creation services available if needed

271952	Valydate Model Creation Services	In the price list but recognized as a service
		Creation of 10 models of any size & complexity (2 pin components at no cost)
		12 months "use it or lose it" scheme
293221	Accelerated Adoption Training	On-site or remote
		Walks customers through their own design to setup & analyze
		Includes a bucket of 100 models (Teams) - 500 models (Enterprise)
271582	On Demand Valydate Review Services	Priced based on design complexity (<20 sheets, >20 sheets >50 sheets, >50 sheets)

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Evaluation feedback (1)

- Using the tool is simple - Verification flow is obvious
  - I quickly browsed through the documentation
- You may have to reformat the customer's BOM so that it can be read by Valydate
- Reading of Cadence Netlist – no issue
- Library management probably requires to spend more time to fully understand all capabilities
- Model development requires to acquire some basic knowledge (e.g. get familiar with the terminology - Pin Type, Pin Treatment…) and some experience but is very doable
  - Modify existing models is certainly the best strategy once you understand how the Search works in the assign model dialog
  - A model is customizable based on the utilization of the component in the design or on the designer's experience
    - Datasheet recommendation capture can be design/utilization-dependent

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Evaluation feedback (2)

- The main difficulty I encountered was the voltage definition despite the helpful “Scan & Detect” functionality
  - A good knowledge of the board is required
  - A schematic of the board as a minimum
  - Hopefully a meaningful net naming can also help
- I did not get it entirely correct after reviewing the settings with the customer but was close
- I showed the customer the results “live” and Valydate was in particular able to detect an unusual usage of some components
  - CUSTOMER was *pleasantly surprised* by the findings

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Next step

- CUSTOMER has acknowledged the relevance of the product !
- They will now get an evaluation license to go further and make their own experience

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Conclusions

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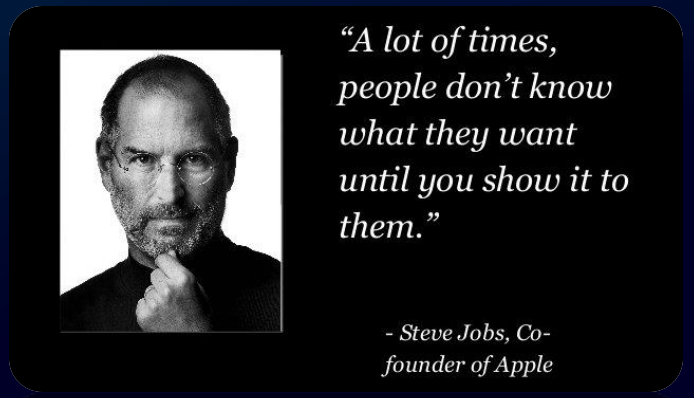
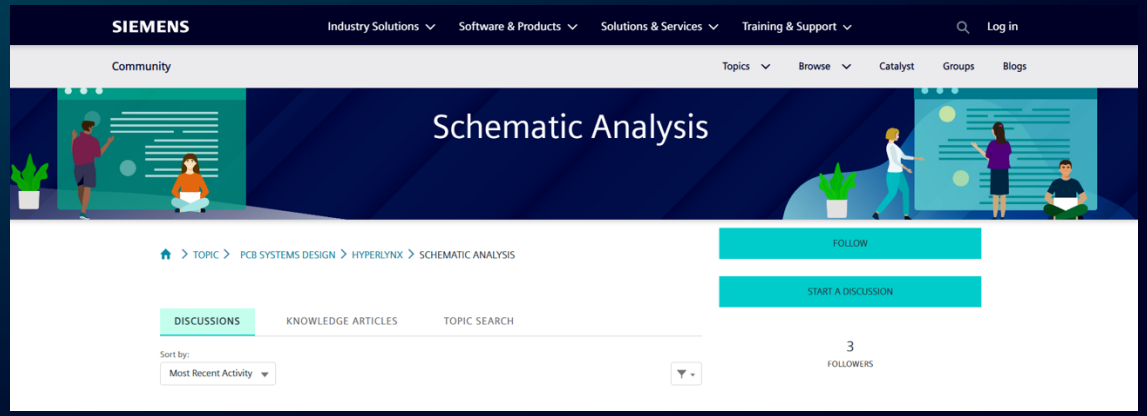
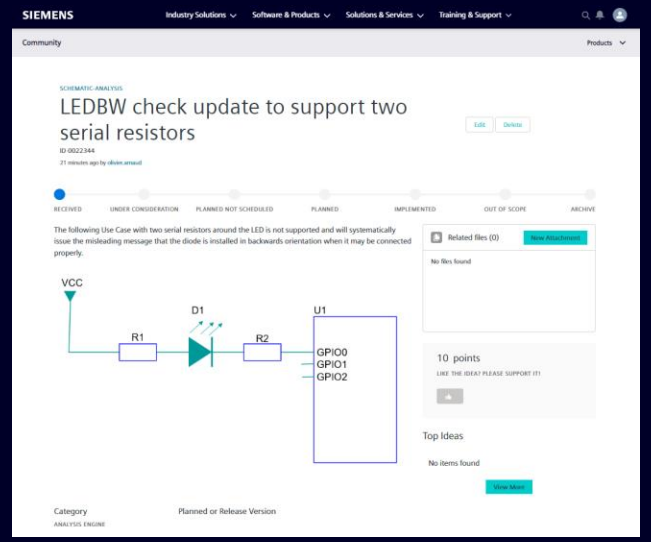
Conclusions (2)

- Customers do not necessary know that Valydate exists in our portfolio
- Valydate adoption is growing
  - A Valydate dedicated Siemens IDEA web page has just been created to post enhancement requests



https://community.sw.siemens.com/s/topic/0TOVb0000000ECfOAM/schematic-analysis





My first Valydate IDEA !

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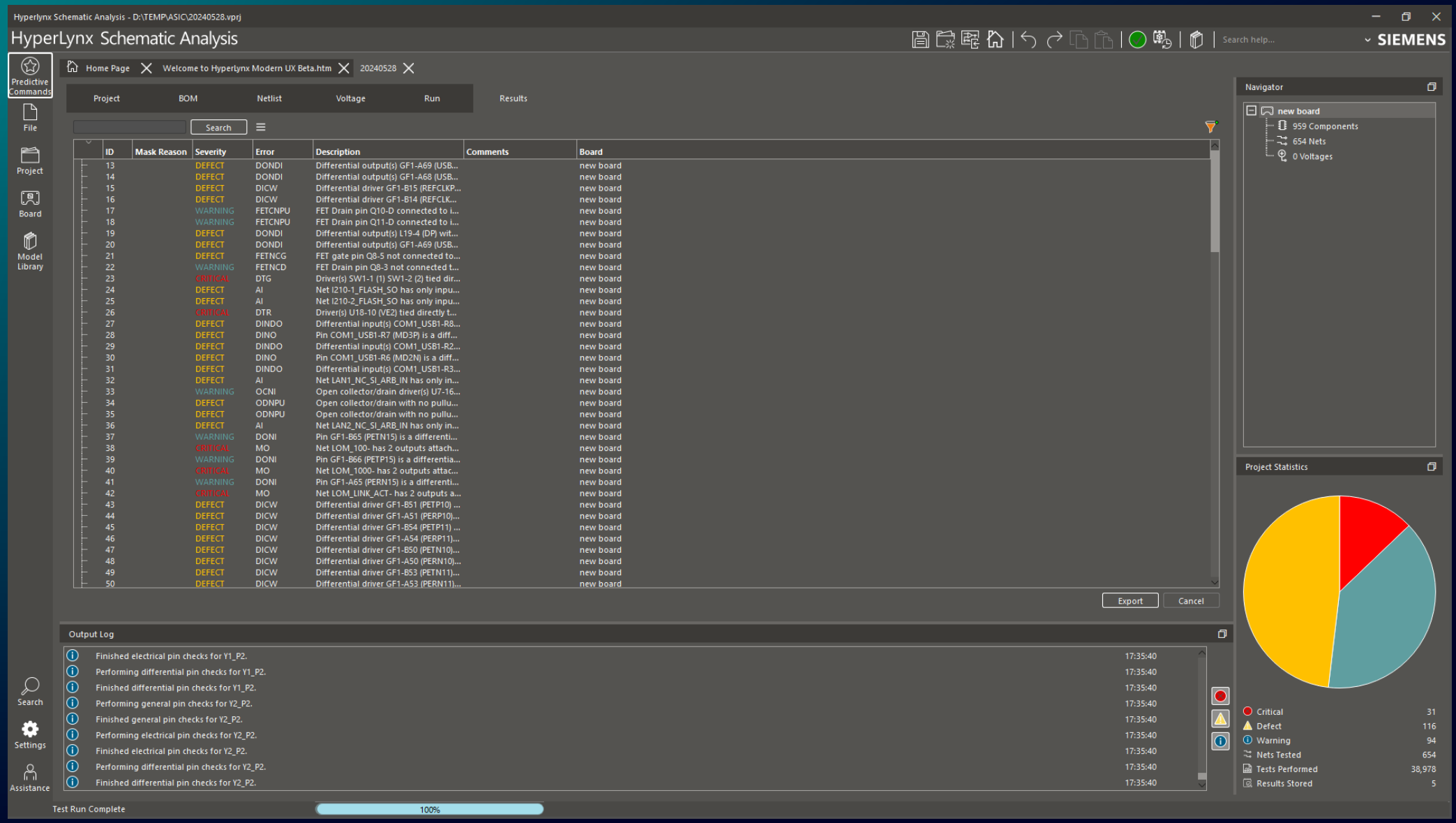
A feel of 2409 – “HyperLynx Schematic Analysis”



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Teşekkür ederim !

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