CDT TECH DAY

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Constraint Manager Tips and Tricks

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Agenda

- General Concepts
- Constraint Manager User Interface
- Routing Order
- Length Constraints
- Clearances
- Differential Pairs
- DDR
- CM and Hyperlynx
- Misc.

General Concepts

What is Constraint Manager?

Constraint Manager (CM) is an integrated, spreadsheet-based interface that is the authoring tool for design intent

Common Constraint Entry environment

- Integrated into the schematic environment
- Integrated into the layout environment
- Cross probing between Constraint Manager and host applications

Complete Constraint Set, always accessible

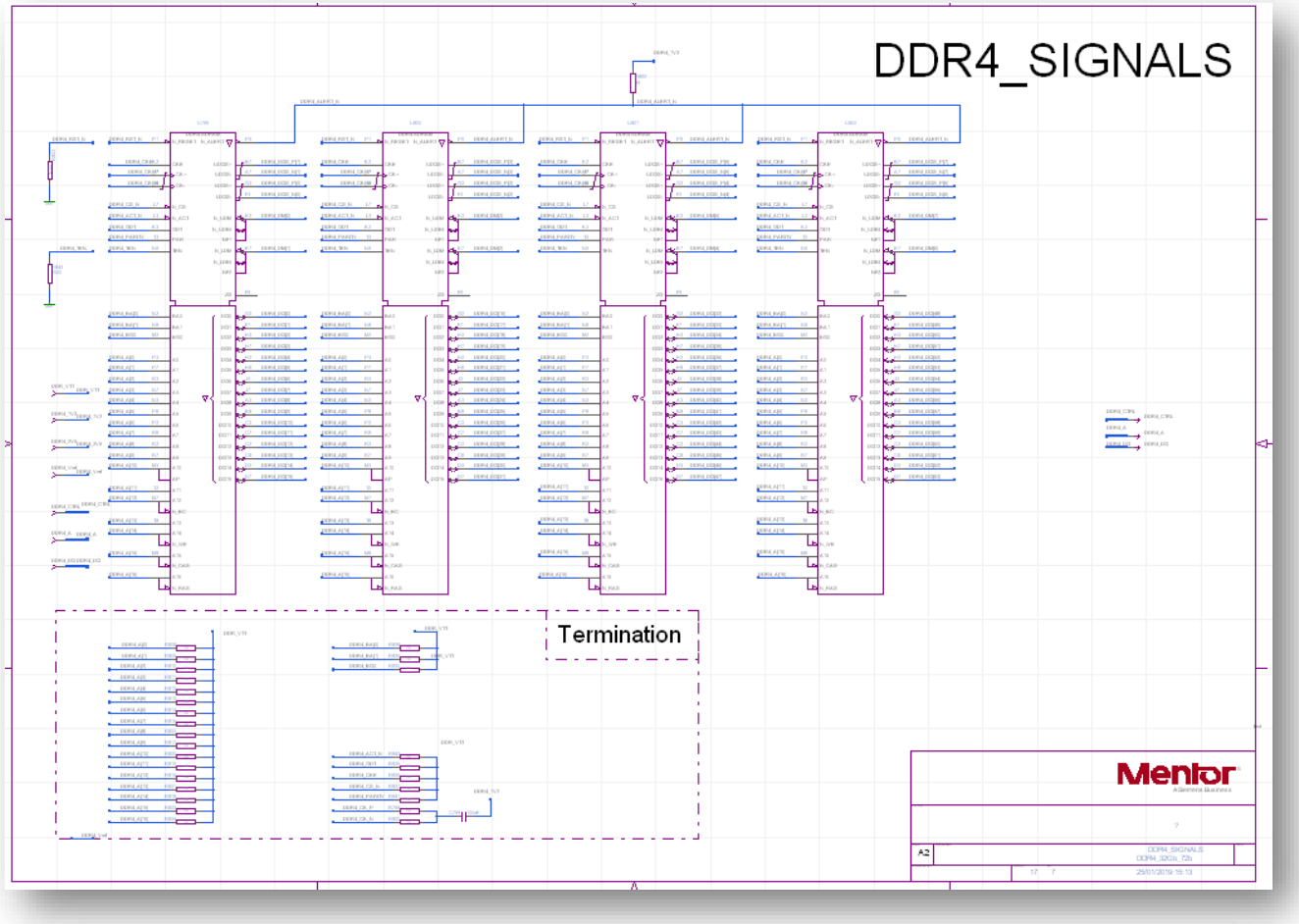
- Constraint Classes control the electrical rules (length, tolerance, stub length, etc..)
- Net Classes control the physical rules (clearances, widths, diff pair spacing, etc.)
- 3D Constraints
- Valor DFM Rule sets

Design Intent on the Schematic

Information that cannot be determined from the Schematic:

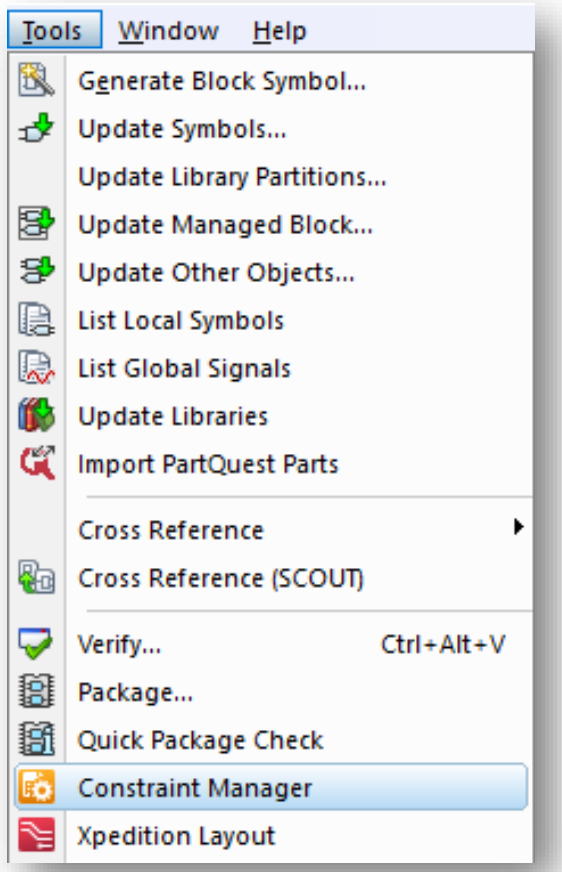
- Routing Lengths
- Routing Widths
- Topology
- Routing Order
- Max Stub Lengths
- Restricted Layers

Constraint Management is needed

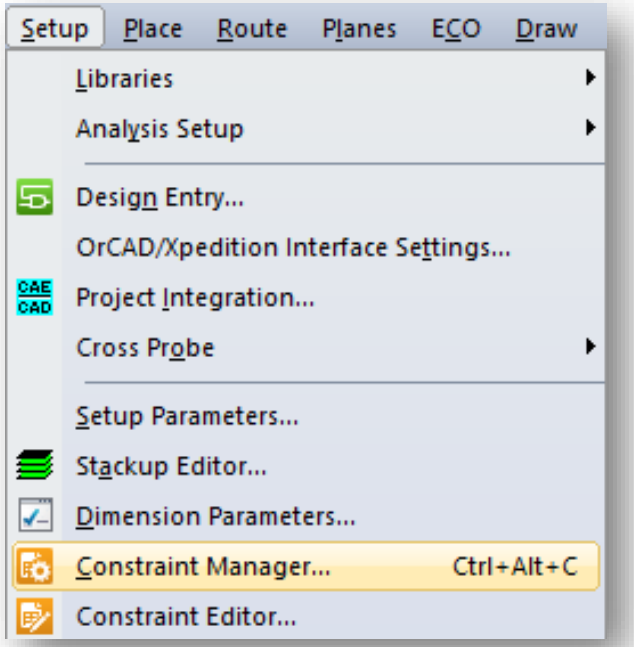


Launching Constraint Manager

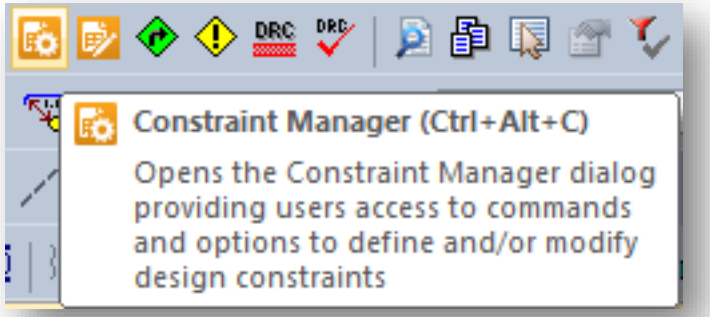
Xpedition Designer: Tools > Constraint Manager



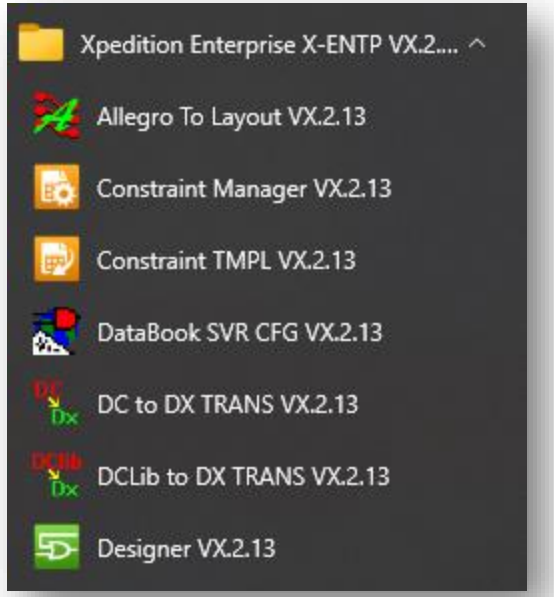
Xpedition Layout: Setup > Constraint Manager



Both Tools: Toolbar Icon



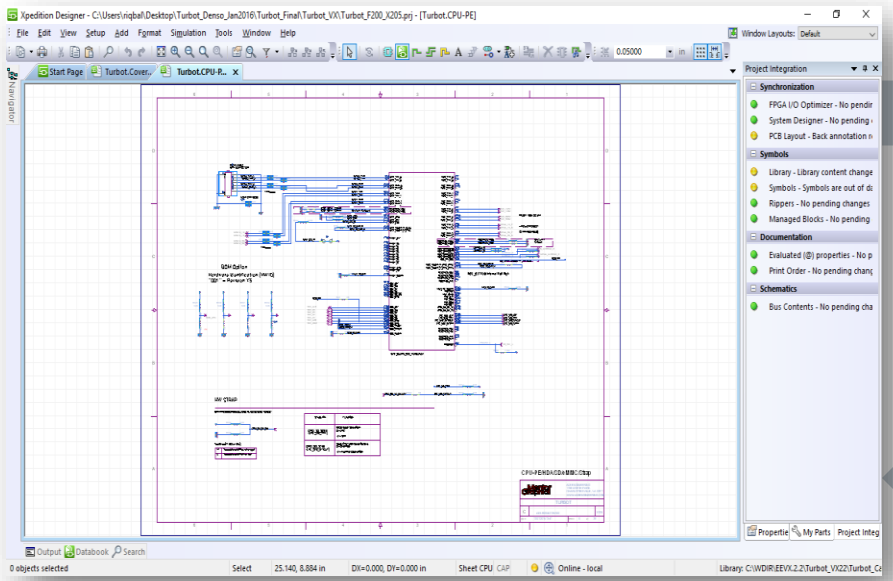
Stand Alone (Start Menu)



How are the front-end & back-end synchronized?

- When Constraints are entered in Designer, you will have to Package and Forward Annotate to promote the changes to Xpedition.
- Constraints entered in Xpedition will be seen in Designer after Back Annotate

Xpedition Designer



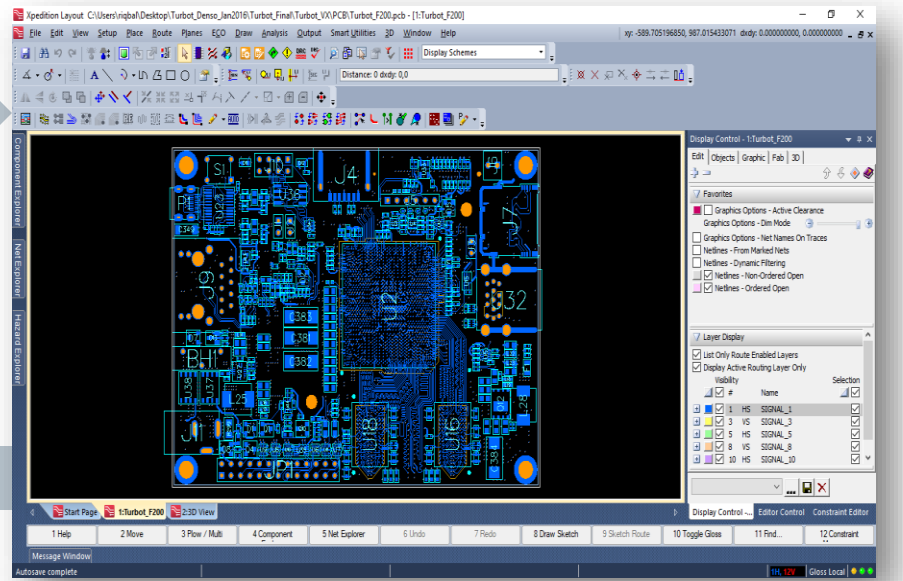
Front-End
Constraint Manager Changes

Package +Forward Annotate

Back-End
Constraint Manager Changes

Back Annotate

Xpedition Layout



Signaling Lights

Xpedition Layout

Schematic connectivity changes are pending

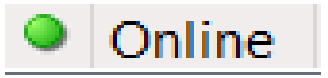
Schematic constraint changes are pending

PCB constraint changes are pending

Click to update Xpedition with CM changes

Schematic & PCB in sync

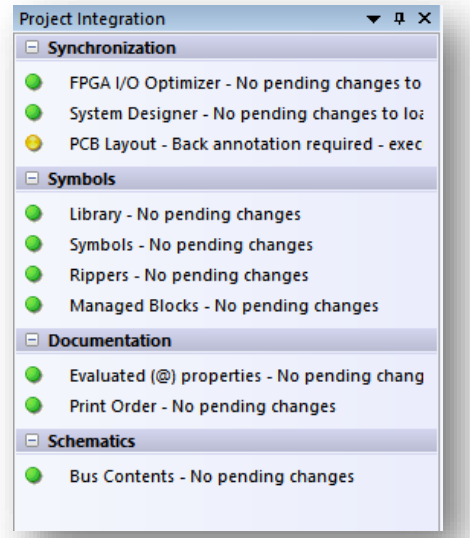
Xpedition Designer

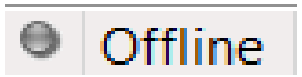


Schematic & PCB in sync

PCB Changes Pending

Click to Open Project Integration





Design is offline

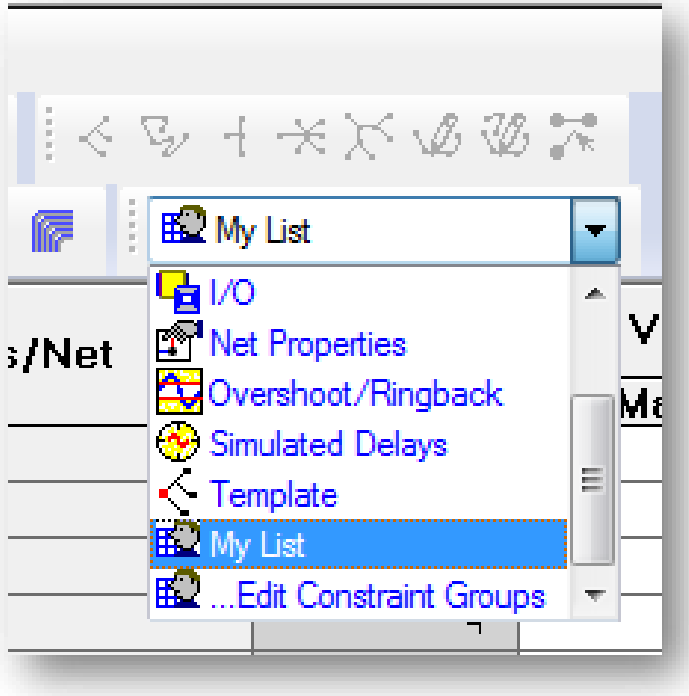
How do I filter the CES columns?

You can filter out the columns that you do not want to see in CES.

There are several predefined Filters

- All
- Delays and Lengths
- Net Properties
- Diff Pair Properties etc..

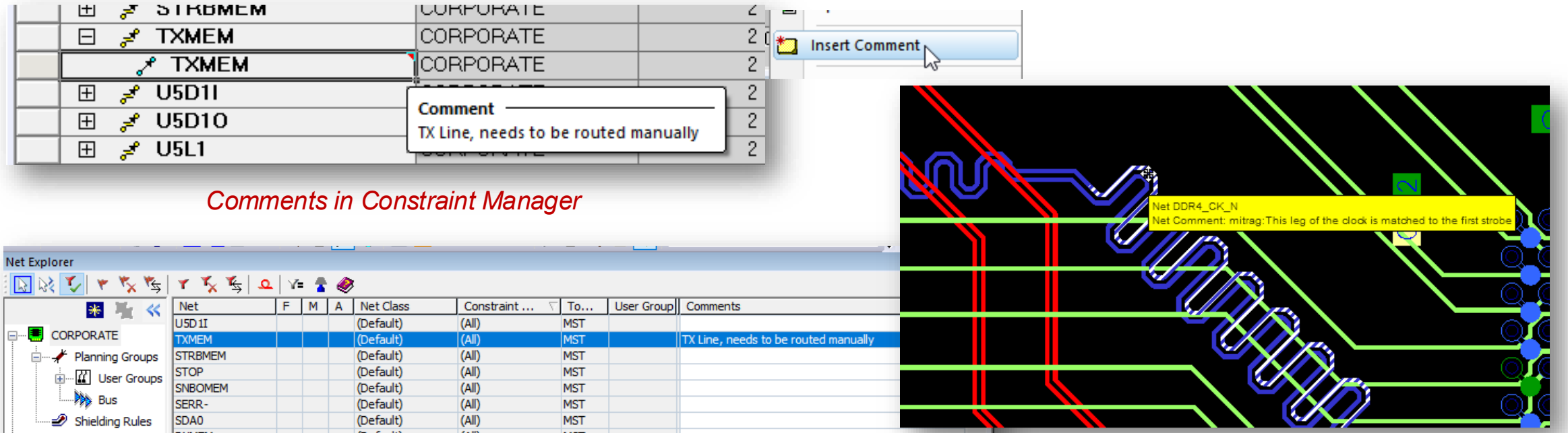
You can create your own filter by choosing “Edit Constraint Groups”



Comments on Nets

Add & display comments to nets from the schematic, constraint manager or layout

- Right Click on a cell and “Insert Comment” in constraint Manager
- Within the layout, comments can be seen on the selected net (View→Toggle Design Tips in Xpedition)
- Within the schematic, the comments would be added to a net and seen within constraint editor add-in UI



Comments in Constraint Manager

Alternative - Comments in Net Explorer

Constraint Manager User Interface

The Net Class Spreadsheet Restricting Layers

Layer Routing Allowed

Routing Width

Single Ended Impedance (Changes trace width)

Differential Impedance

Distance between P and N sides of Pair

Set Diff pair Via spacing

Scheme/Net Class/Layer	Route	Trace Width (th)			Typical Impedance (Ohm)	Differential		
		Minimum	Typical	Expansion		Typical Impedance (Ohm)	Spacing (th)	Via Spacing
DDR4_SE_CMD_ADDR	☑	4	4	6			9.843	20
DDR4_DIFF_DQS	☑	4	4	6			9.843	20
DDR4_DIFF_CLK	☑	4	4	6	4		9.843	20
SerDes_100ohm	☑	4	4	6			9.843	20
TOP	☐	4	4	6	59.299..	113.53..	9.843	20
GND1	☐	4	4	6			9.843	20
SIGNAL_2	☐	4	4	6	48.212..	95.126..	9.843	20
SIGNAL_3	☐	4	4	6	52.238..	98.778..	9.843	20
POWER1	☐	4	4	6			9.843	20
GND2	☐	4	4	6			9.843	20
SIGNAL_4	☑	4	4	6	51.752..	97.973..	9.843	20
SIGNAL_5	☑	4	4	6	48.261..	95.229..	9.843	20
GND3	☐	4	4	6			9.843	20
BOTTOM	☐	4	4	6	59.869..	114.485..	9.843	20
(Minimum)								
(Default)		4	4	6			9.843	20

Restricted layers

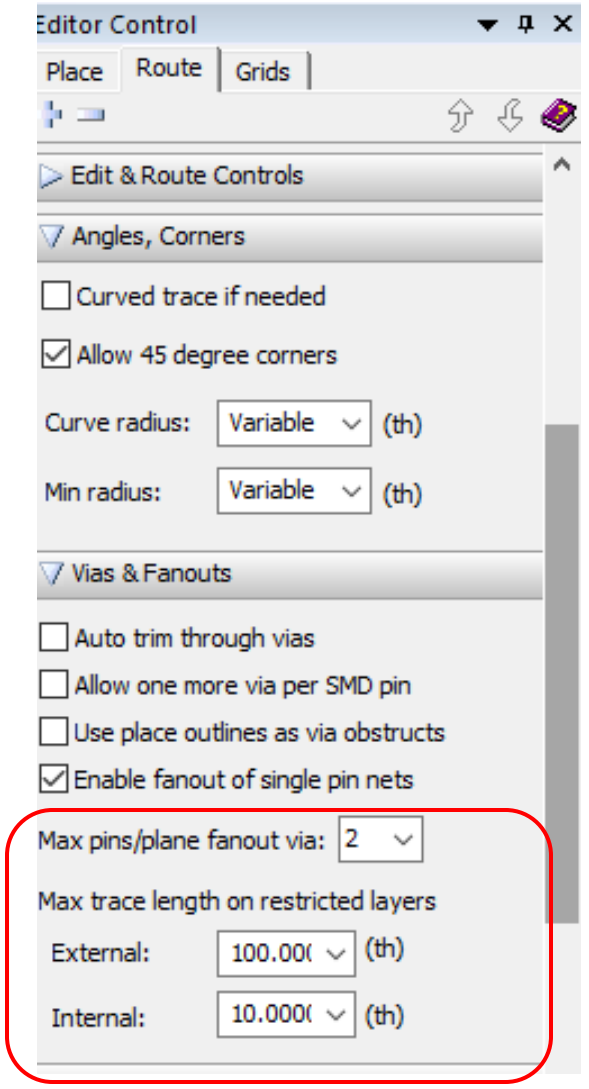
Restricted Layers: Max Internal and External

- Controls how much routing is allowed on a restricted layer
- Most Common use – Fanout nets

Scheme/Net Class/Layer	Route	Trace Width (th)			Typical Impedance (Ohm)	Differential		
		Minimum	Typical	Expansion		Typical Impedance (Ohm)	Spacing (th)	Via Spacing
DDR4_SE_CMD_ADDR	☑	4	4	6			9.843	20
DDR4_DIFF_DQS	☑	4	4	6			9.843	20
DDR4_DIFF_CLK	☑	4	4	6	4		9.843	20
SerDes_100ohm	☑	4	4	6			9.843	20
TOP	☐	4	4	6	59.299..	113.53..	9.843	20
GND1	☐	4	4	6			9.843	20
SIGNAL_2	☐	4	4	6	48.212..	95.126..	9.843	20
SIGNAL_3	☐	4	4	6	52.238..	98.778..	9.843	20
POWER1	☐	4	4	6			9.843	20
GND2	☐							
SIGNAL_4	☑							
SIGNAL_5	☑							
GND3	☐							
BOTTOM	☐	4	4	6	59.869..	114.485..	9.843	20
(Minimum)								
(Default)		4	4	6			9.843	20

These Nets can still route on the outer layers, up to 200 mils

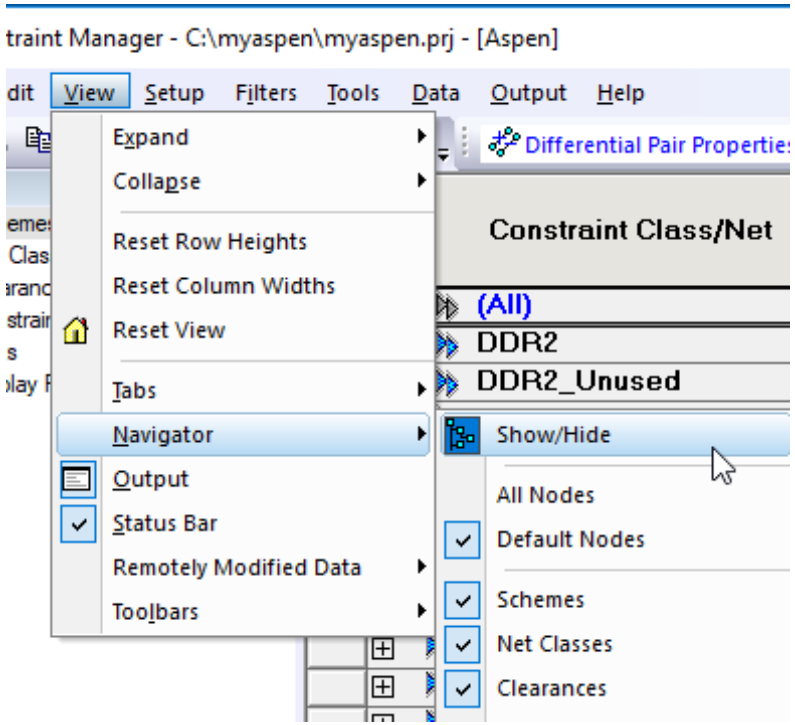
Restricted Layer Length (th)			
Max External	*Actual External*	Max Internal	*Actual Internal*
200.000		200.000	

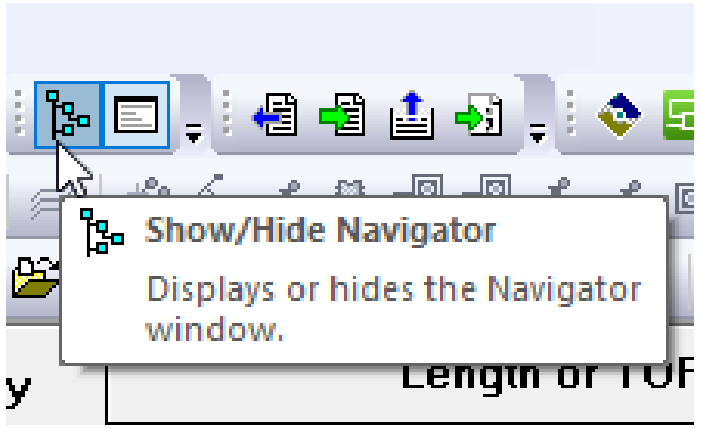


The Navigator

- The Navigator provides a hierarchical view of all of different sections of Constraint Manager

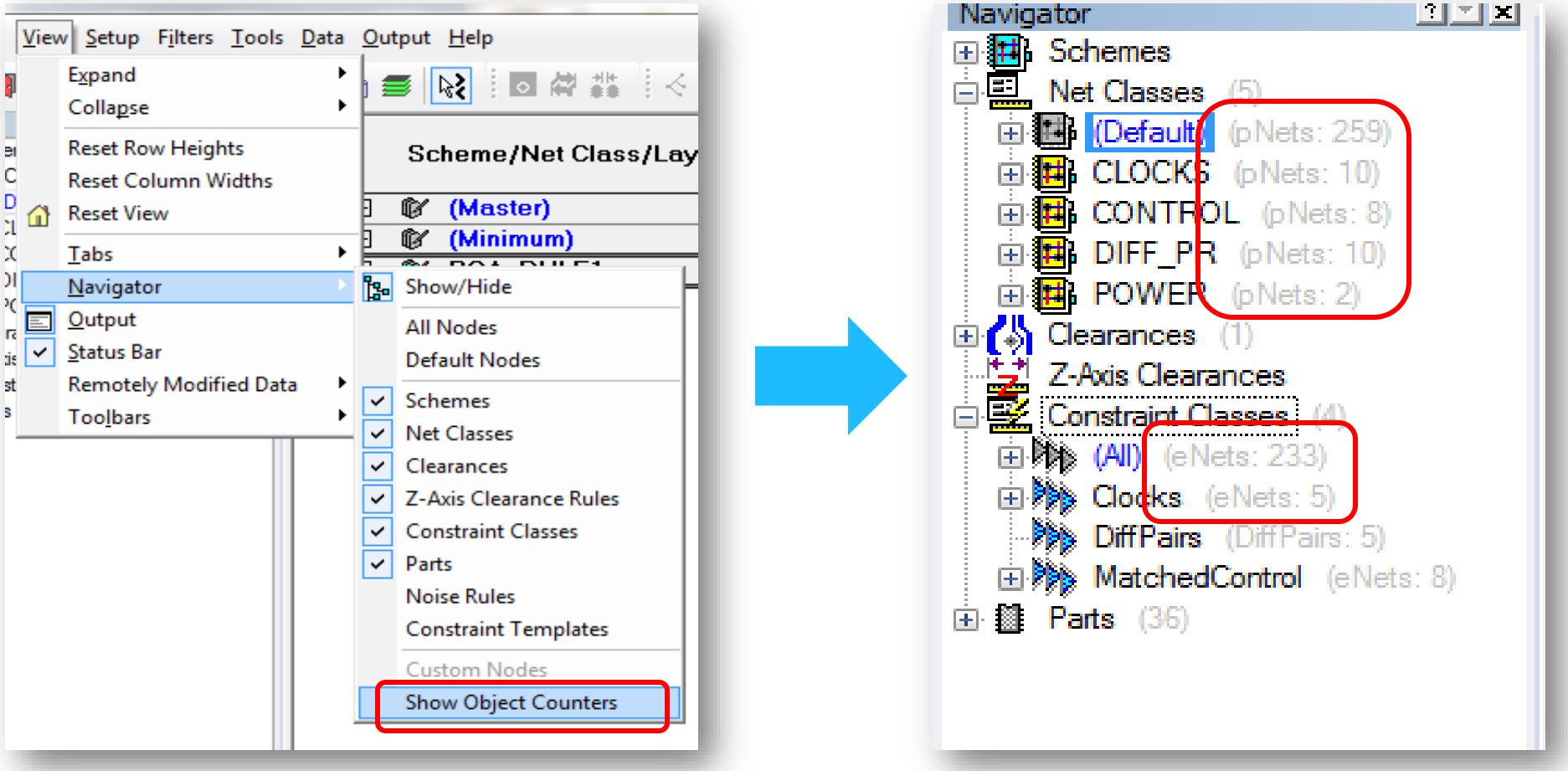
- View→Navigator→Show/Hide





Quantity of nets per class in the Navigator

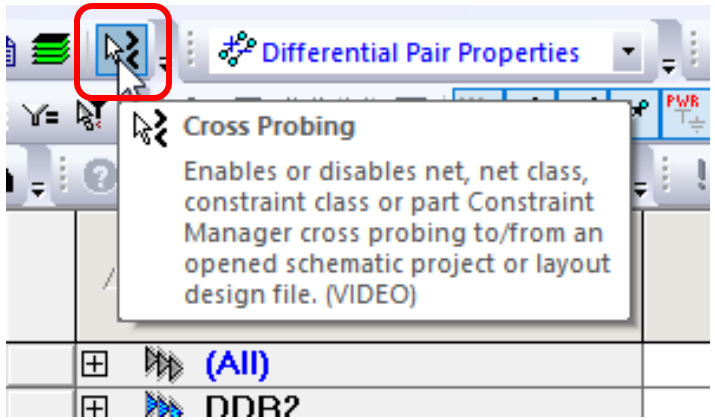
- From the View > Navigator > Show Object Counters menu
- Useful for finding empty net classes



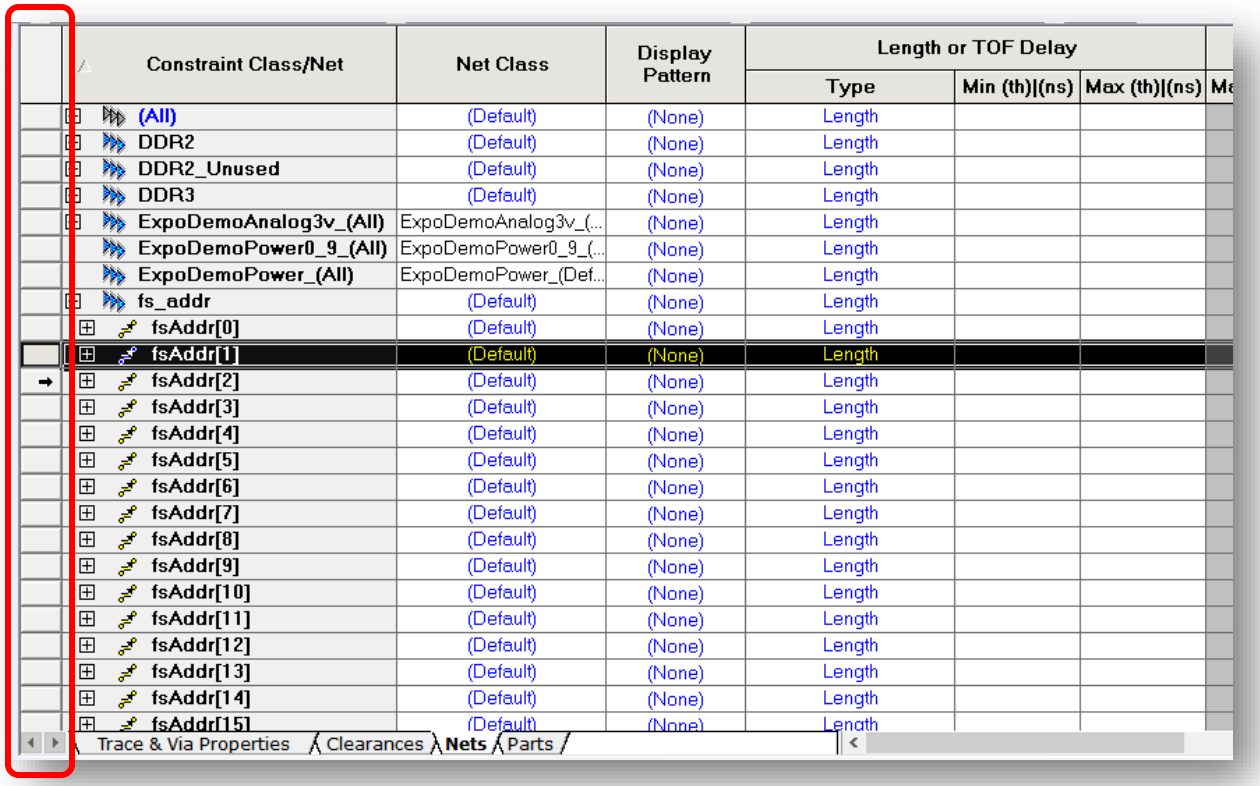
The Cross Probe Column

It is **highly recommended** that you enable “Cross Probing”

- Selecting a net or part will cross probe to Xpedition (r designer)
- Highlights the entire row making it easier to follow across the spreadsheet



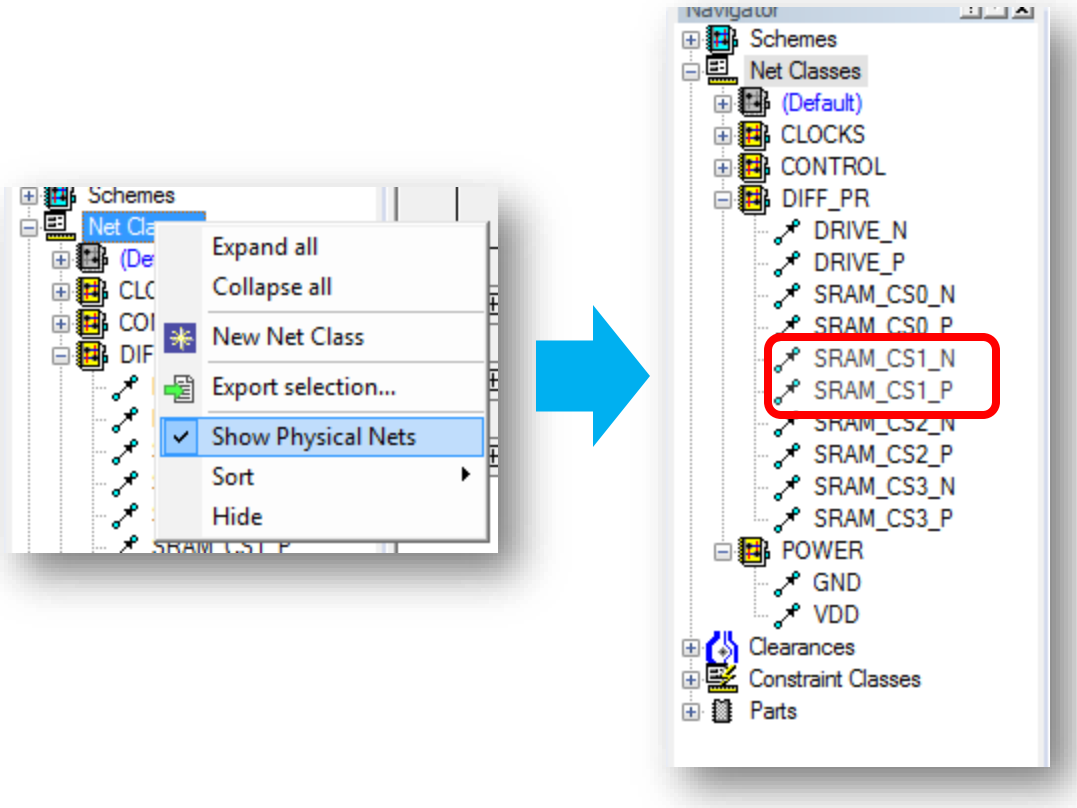
Cross Probe Column



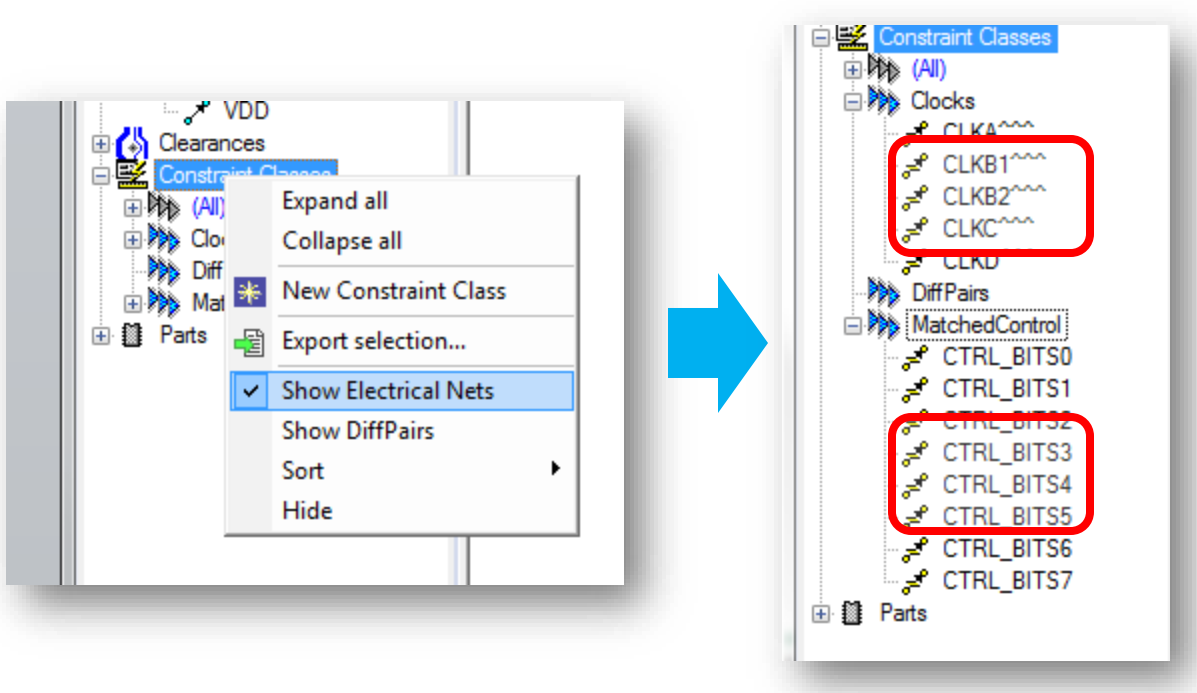
View net names in the Navigator

Right Click to “Show Physical Nets” or “Electrical Nets” if you would like to see the net names belonging to a class in the navigator.

Net Classes



Constraint Classes



Change Rules on a top level row

Whenever you modify a constraint on a row that has sub-rows (Rows that inherit a higher rows values), you will be prompted to confirm that you want this constraint propagated.

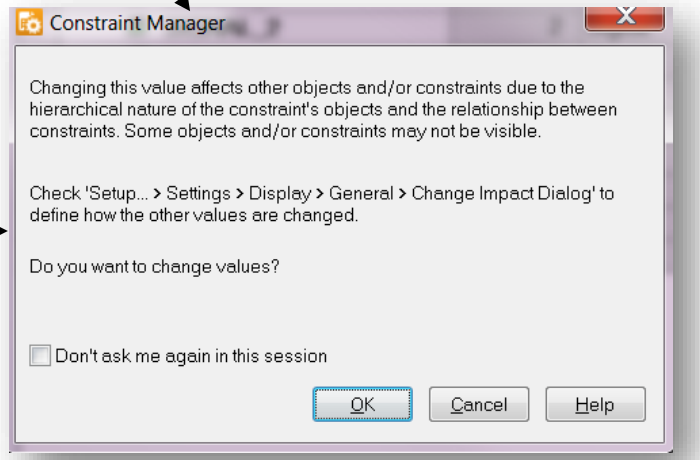
Changing a rule on this row

Affects the rows below it in the hierarchy

CM asks you if you are sure that you want to affect all lower level rows

Check this if you do not want to be prompted every time

Scheme/Clearance Rule/Layer	Index	Type	Trace To		
			Trac	Pad (	Via
(Master)					
(Default Rule)			0.007	0.007	0.007
4mil			0.007	0.007	0.007
PHYSICAL_1	1	Signal	0.005	0.006	0.007
AGND	2	Power	0.007	0.007	0.007
P15V	3	Power	0.007	0.007	0.007
M15V	4	Power	0.007	0.007	0.007
PHYSICAL_5	5	Signal	0.005	0.006	0.007
PHYSICAL_6	6	Signal	0.007	0.007	0.007
8mil			0.009	0.007	0.007
PHYSICAL_1	1	Signal	0.008	0.007	0.007
AGND	2	Power	0.008	0.007	0.007
P15V	3	Power	0.008	0.007	0.007
M15V	4	Power	0.008	0.007	0.007
PHYSICAL_5	5	Signal	0.008	0.007	0.007
PHYSICAL_6	6	Signal	0.007	0.007	0.007
+5V			0.007	0.007	0.007



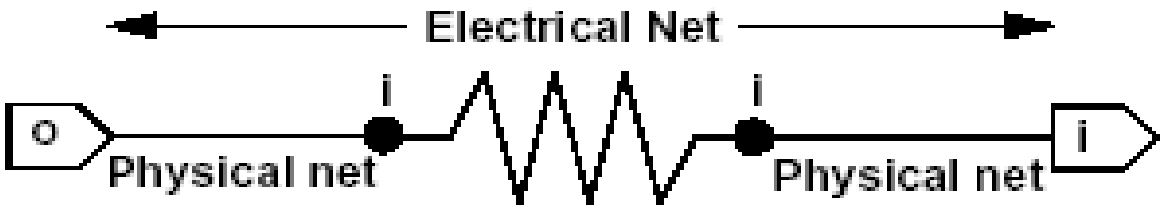
Physical and Electrical Nets

Physical Net

- Most commonly named as “net”
- Connects physical pins

Electrical Net

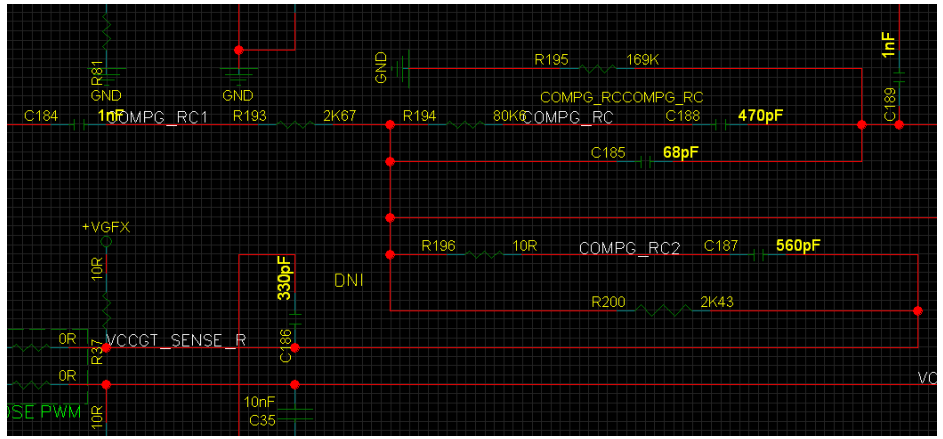
- The electrical connectivity of signals through a series device
- Two or more Physical Nets that connect through a series device (discrete or resistor packs)
- Electrical Net Name -First name at the top with “^^^” appended to the net name
- CM Automatically sums both sides of the electrical net for delay rules



Analog Nets

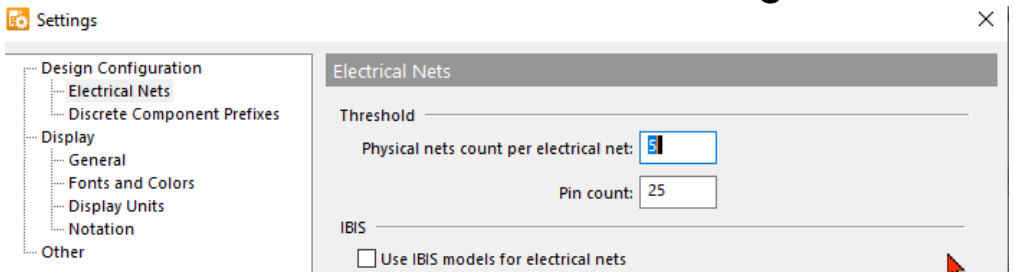
Analog nets will get merged into one large electrical net because of the discrete parts in the circuit. Check the “Analog” button to split them into their individual nets:

Analog Net.



	Constraint Class/Net	Analog
	(Custom...)	
⊟	$1N201^^^	☐
	$1N201	☐
	$1N206	☐

Can limit Electrical nets from Designer/Constraints

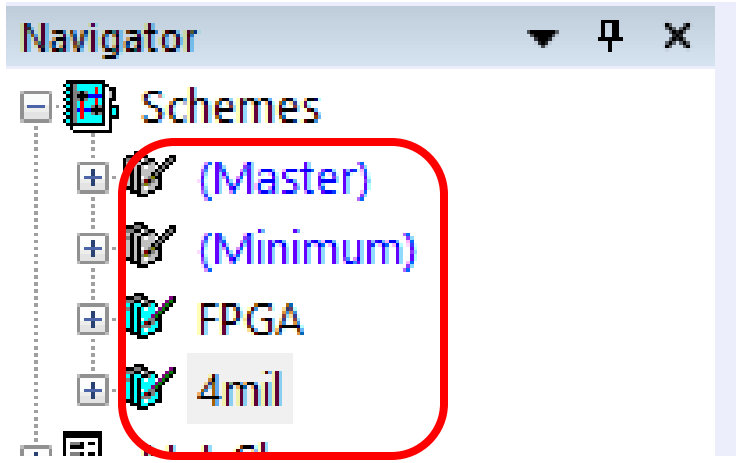


	Constraint Class/Net	Analog
	(Custom...)	
⊞	$1N201	☑
⊞	$1N206	☑

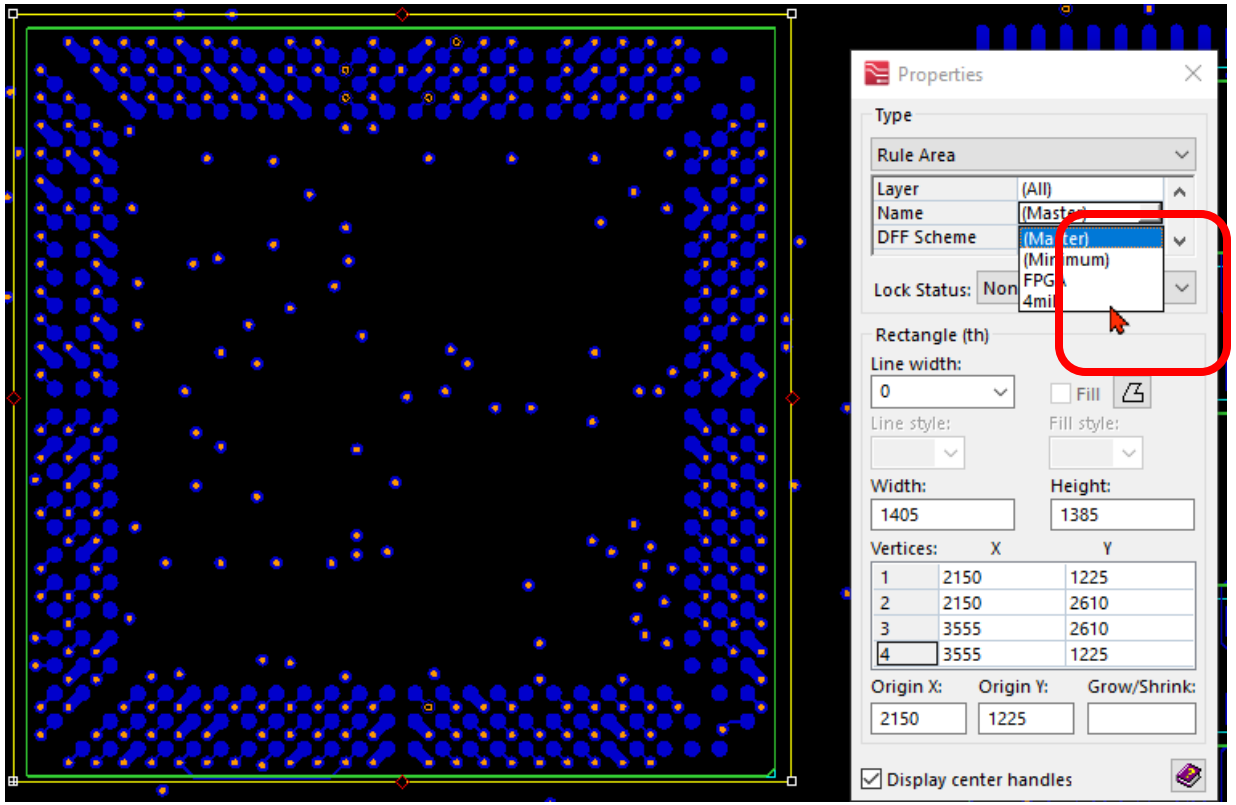
What are Schemes and Rule Areas?

A Scheme is a unique set of physical clearance rules (e.g. 4 mil line and spacing)
A Rule Area if an area in Xpedition that defines where a scheme is to take effect.
The Master Scheme is used when no rule area is defined.

Schemes in CM



Rule Areas in Xpedition



Constraint Class vs. Net Class

What are Net Classes?

Net Classes are groups of nets that control the physical routing parameters like:

- Trace width
- Differential spacing, impedance
- Layer restrictions
- Via assignments
- Clearances

Scheme/Net Class/Layer	Via Assignments	Route	Trace Width (th)			Typical Impedance (Ohm)	Differential	
			Minimum	Typical	Expansion		Typical Impedance (Ohm)	Spacing (th)
BGA								
(Default)	(default)	☑	3.000	4.000	5.000			10.000
FADDR	(default)	☑	3.000	4.000	5.000			10.000
CLOCKS	(default)	☑	5.000	6.000	8.000	50.000	100.000	10.000
DP_100_OHM	(default)	☑	4.000	5.000	8.000			7.000
CLOCK2	(default)	☑	5.000	6.000	8.000	50.000	100.000	10.000
PWR_020_MIL	(default)	☑	8.000	20.000	25.000			10.000
BSYNC	(default)	☑	5.000	6.000	8.000	50.000	100.000	7.000
FDATA	(default)	☑	3.000	4.000	5.000			10.000

What are Constraint Classes?

Constraint Classes are groups of nets that control Electrical constraints

- Trace length
- Topology
- Stub length
- Diff pair tolerance

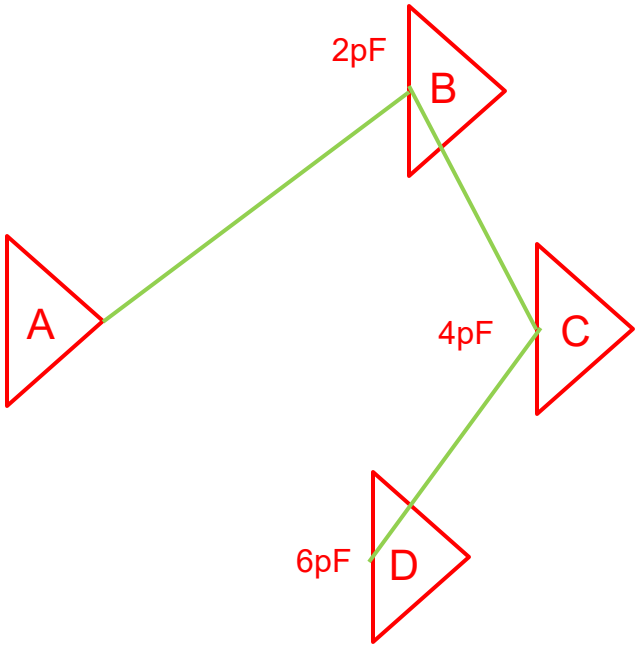
Constraint Class/Net	# Pins	Topology	Power Net	Stub Length (th)		# Vias		Backdrill	Restricted Layer Length (th)			
		Type		Max	*Actual*	Max	*Actual*		Max External	*Actual External*	Max Internal	*Actual Internal*
⊟ BSYNC		MST		300.000				☐				
⊟ BSYNC+,BSYNC-	8	Custom		1,000.00				☐				
⊞ BSYNC+	4	Custom		1,000.00				☐				
⊞ BSYNC-	4	Custom		1,000.00				☐				

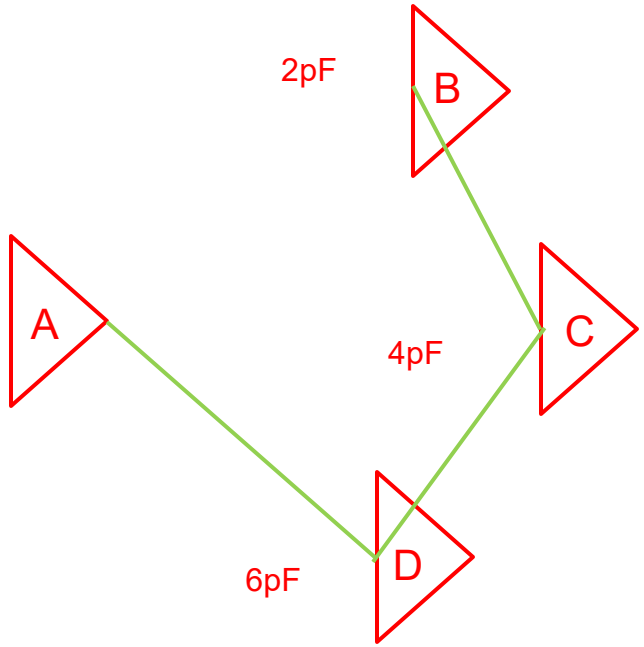
Routing Order

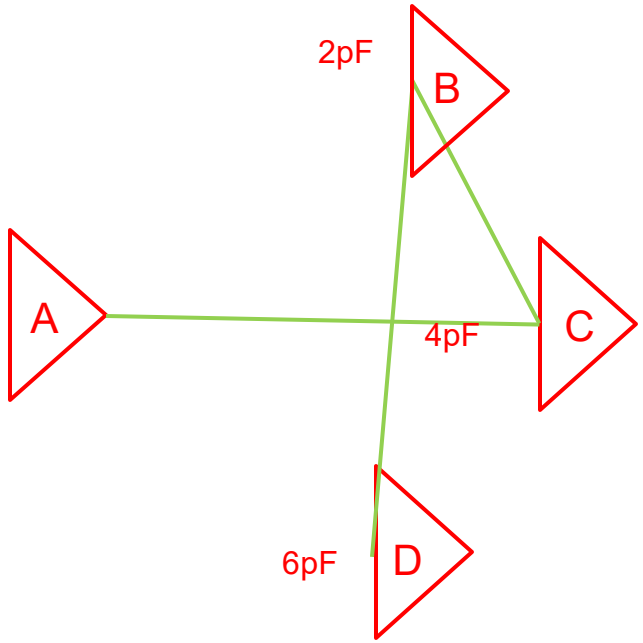
Topology and Order

- Topology generally refers to the arrangement netlines and subsequently the routing.
- “Order” refers to the sequence that the pins on a net need to be routed.

  Example: All three examples have “Chained” topology, but each has a different order







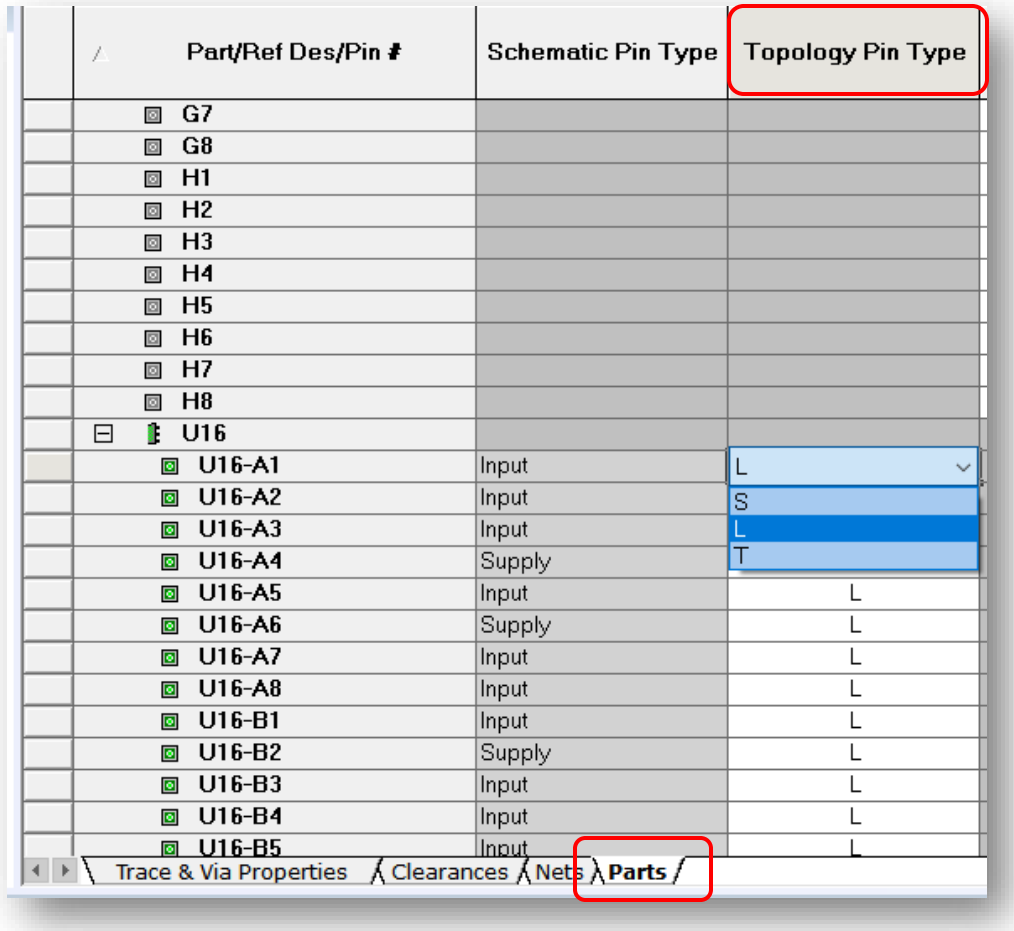
Topology Pin Type

- Built in Topologies are highly dependent on the pin type.
- S (Source) or L (Load) (Bidirectional becomes an S)
- Inherited from the Designer symbol pin type
- You can override the default pin type on the Parts tab:

Part/Ref Des/Pin #	Schematic Pin Type	Topology Pin Type
19		
20		
U16		
U16-1	Input	L
U16-2	Tristate	S
U16-3	Input	L
U16-4	Input	L
U16-5	Tristate	S
U16-6	Tristate	S
U16-7	Input	L
U16-8	Input	L
U16-9	Tristate	S
U16-10	Supply	
U16-11	Input	L
U16-12	Tristate	S
U16-13	Input	L
U16-14	Input	L

Net Topologies and Pin Type

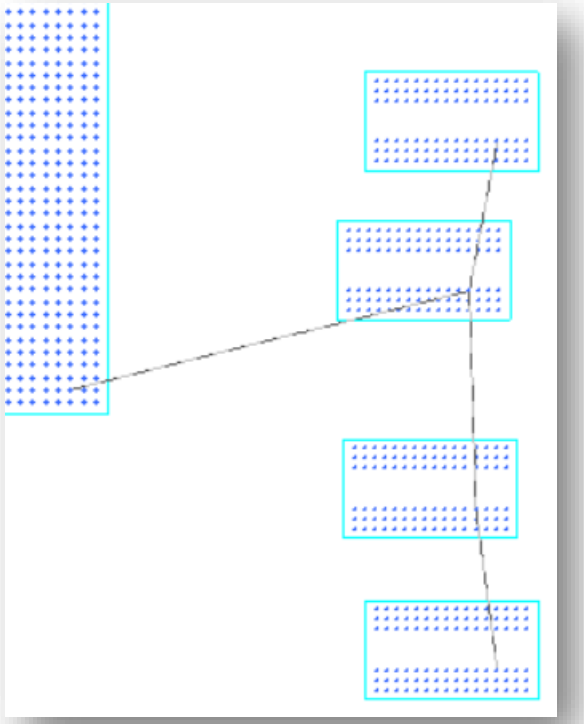
- The Standard Topologies are dependent on the Pin Type (Source, Load, Termination)
- You can override the pin type on the Parts Tab/Topology Pin Type Columns

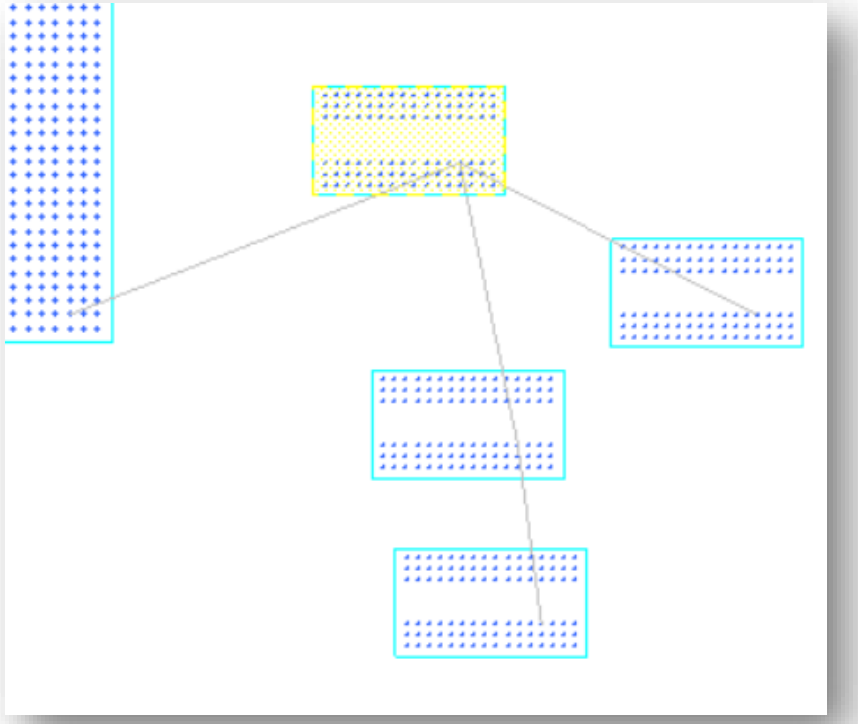


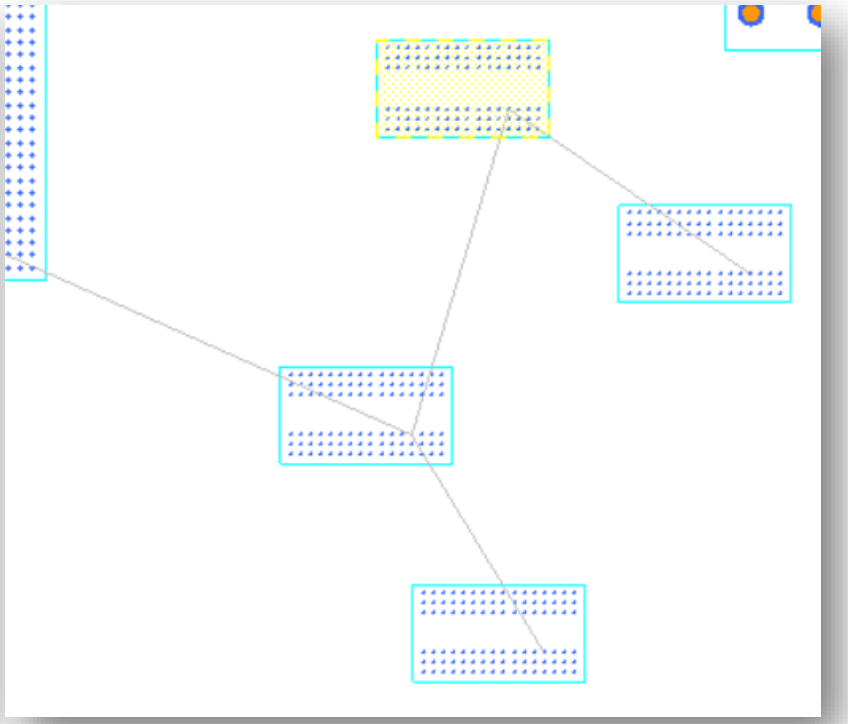
Net Topologies - MST

- Minimum Spanning Tree – netlines follow the shortest path based on the placement
- S,L (Pin Types) are ignored
- Set Netline Optimization to be full in Editor Control.

Note as parts are moved around to the MST topology changes to minimize the netline lengths



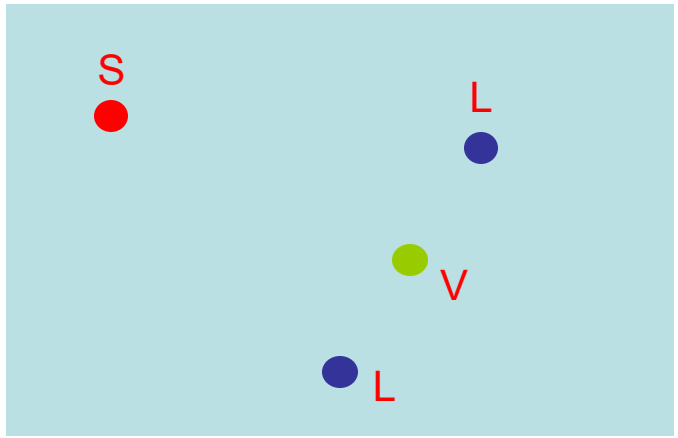


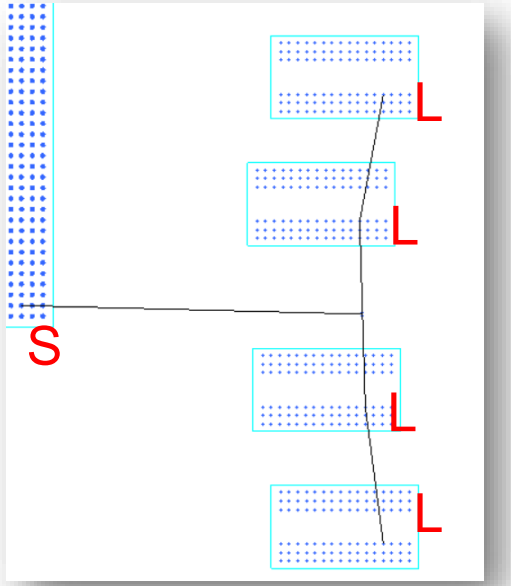


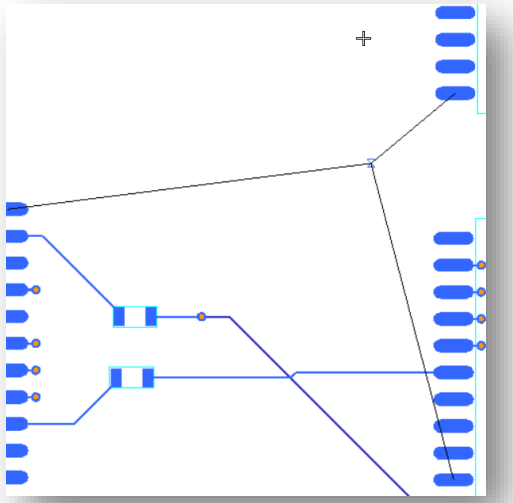
Net Topologies T-Shape

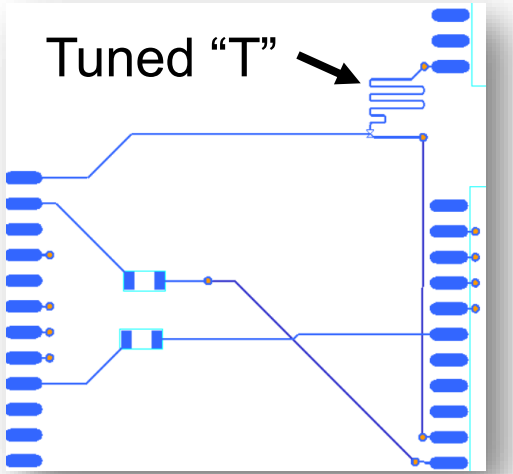
T-Shape

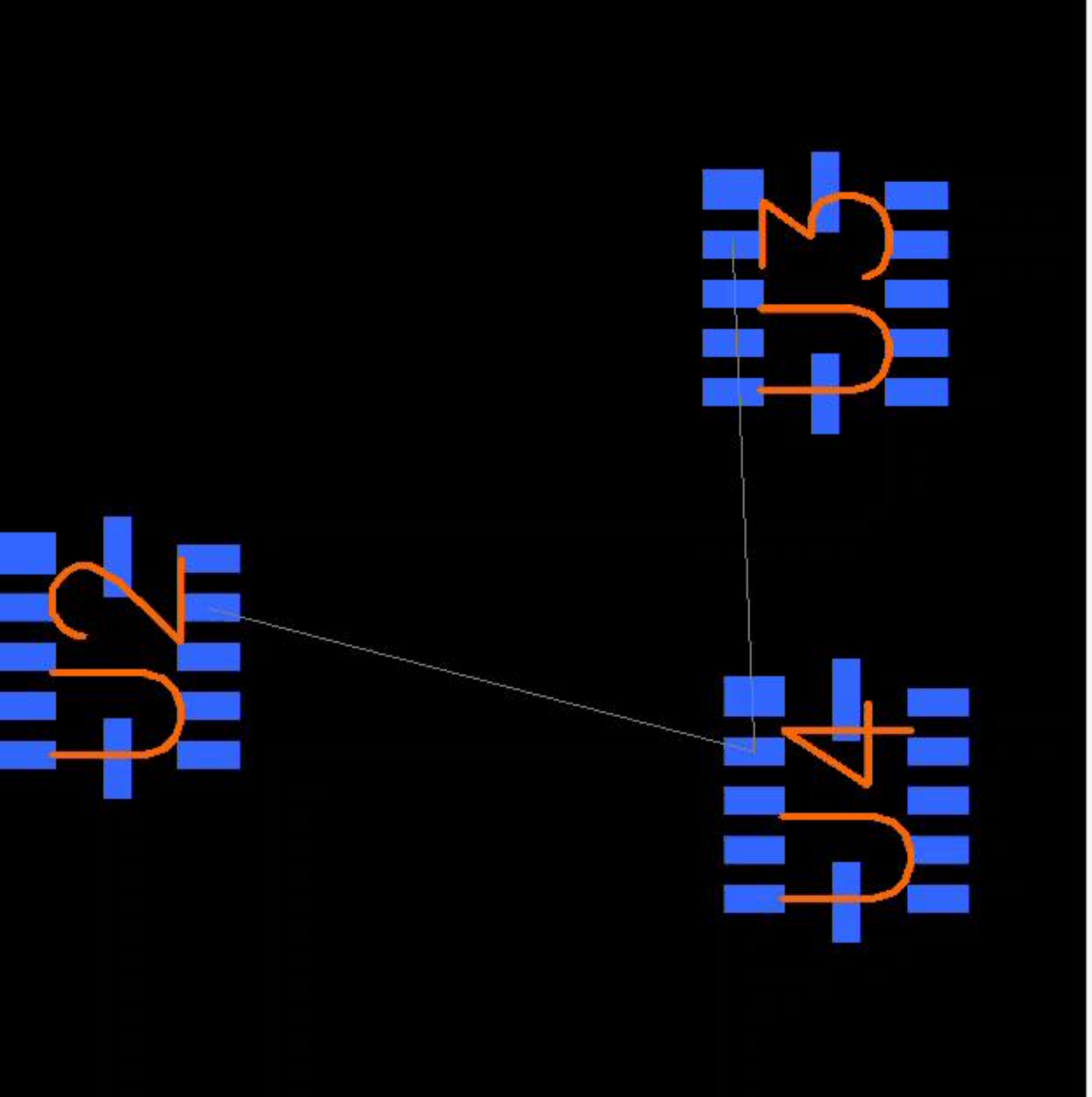
- From source to 2 or more loads
- Each load is “understood” to be equal or balanced, no other constraint is required. (You do not have to put a matched length rule in for the two legs of the “T”)
- Virtual Pin located mid-way between the loads
- The virtual pin can be moved in Xpedition











CLK_IN_$3I553	MST
CLK_IN_$3I554	MST
CLK_IN_$3I555	MST
CLK_IN_$3I556	MST
CLK_IN_$3I658	MST
CLK_IN_$3I659	MST
CLK_IN_$3I753	MST
CLK_IN_DigitalPotSwitches548	MST
CLK_IN_DigitalPotSwitches548Switches657	MST
clk_tree	MST
CLKOUT	MST
Data(0)	MST
Data(1)	MST
Data(2)	MST
Data(3)	MST
Data(4)	MST
Data(5)	MST
Data(6)	MST
Data(7)	MST
Data(8)	MST
Data(9)	MST

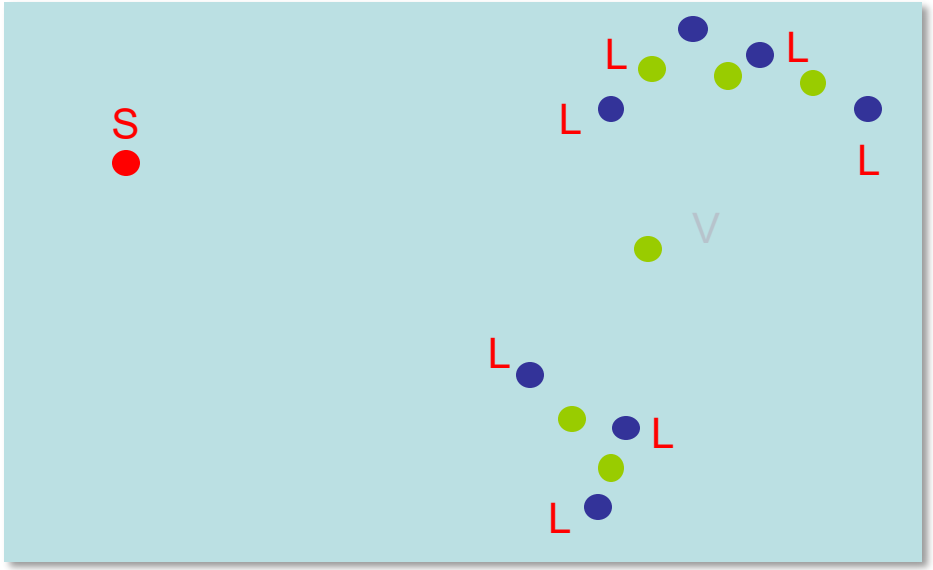
Via Properties | Clearances | Nets | Parts | Constraint Templates

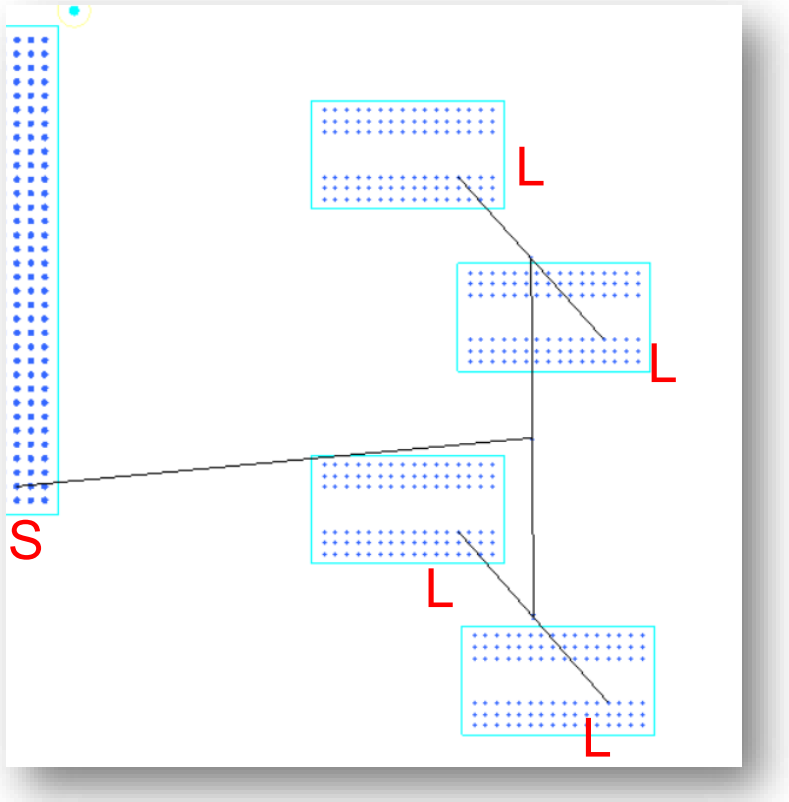
ns either all load pins or all source pins. Until some pin type changes are made, the t

Net Topologies - H-Tree

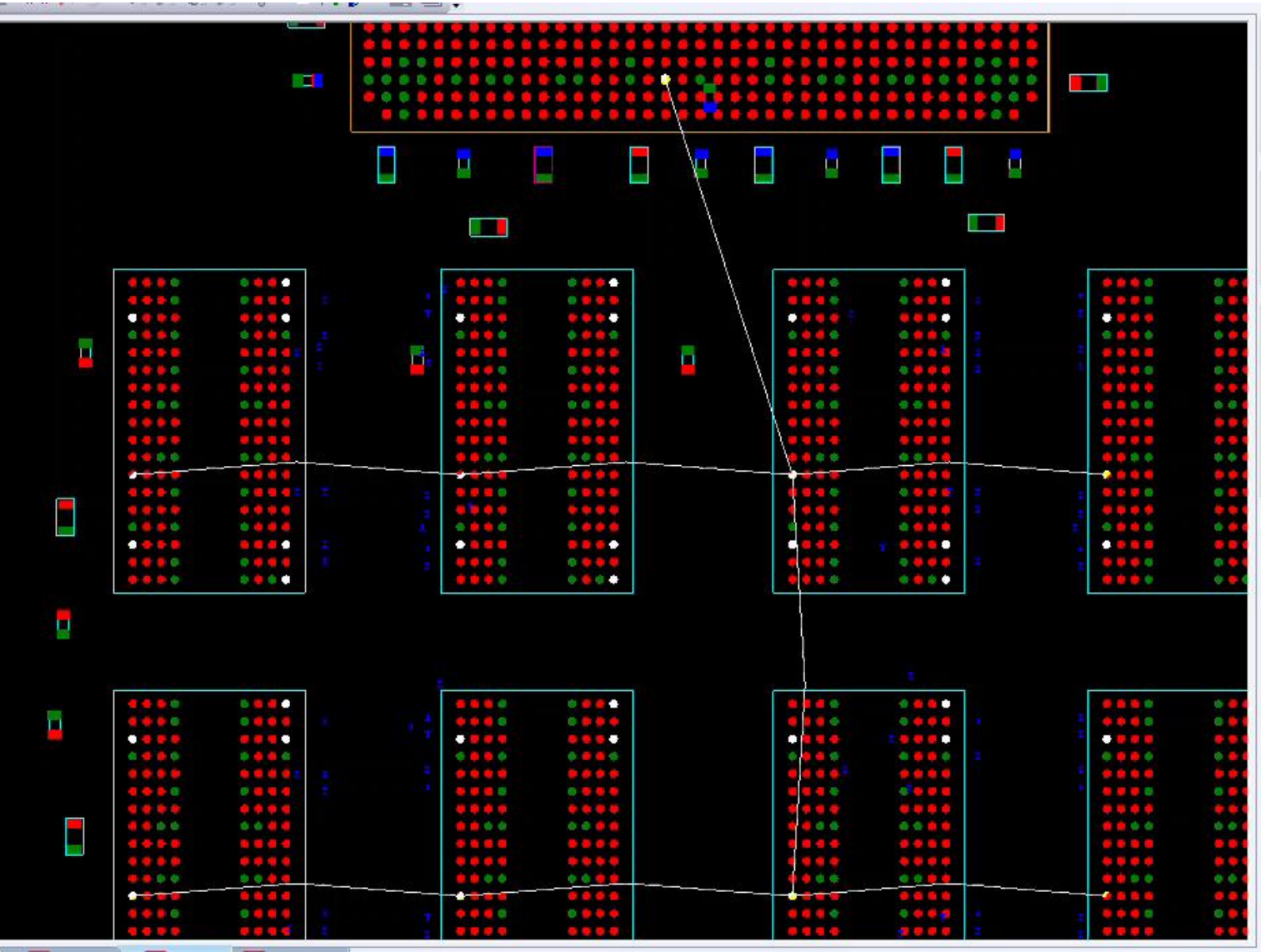
Uses multiple virtual pins to balance the loads forming a hierarchical tree model

- Virtual pin placed at the mid-point of each pair to balance lengths





H Tree Video

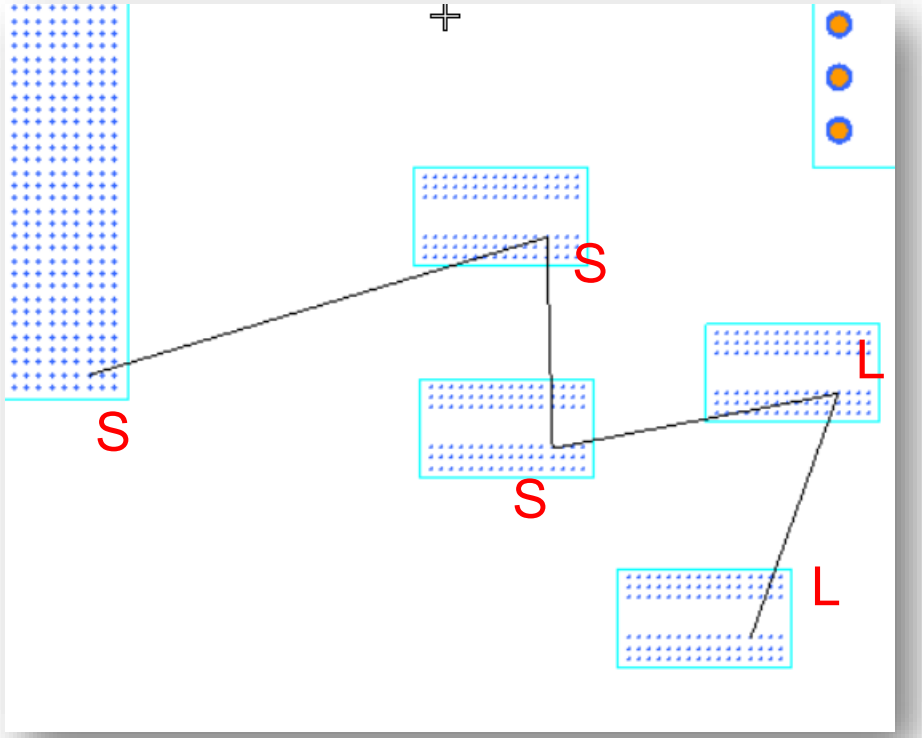


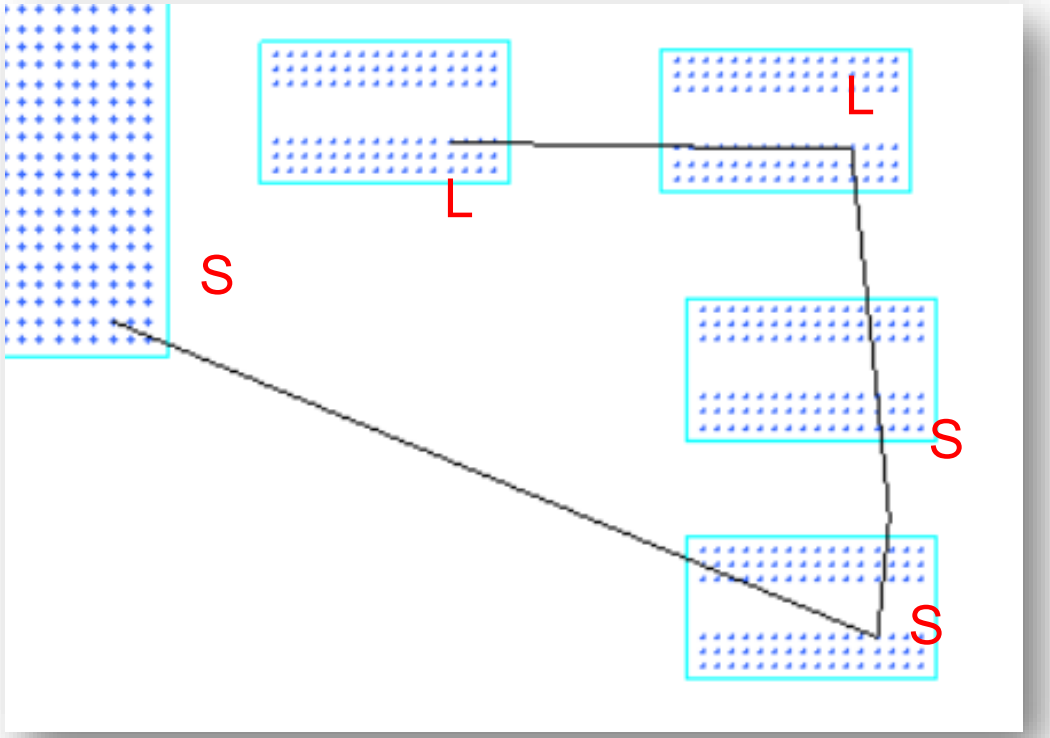
Constraint Class/Net	Type	Net Class
Address	MST	(Default)
RLDRAM_ADDRESS0	MST	(Default)
RLDRAM_ADDRESS1	MST	(Default)
RLDRAM_ADDRESS2	MST	(Default)
RLDRAM_ADDRESS3	MST	(Default)
RLDRAM_ADDRESS4	MST	(Default)
RLDRAM_ADDRESS5	MST	(Default)
RLDRAM_ADDRESS6	MST	(Default)
RLDRAM_ADDRESS7	MST	(Default)
RLDRAM_ADDRESS8	MST	(Default)
RLDRAM_ADDRESS9	MST	(Default)
RLDRAM_ADDRESS10	MST	(Default)
RLDRAM_ADDRESS11	MST	(Default)
RLDRAM_ADDRESS12	MST	(Default)
RLDRAM_ADDRESS13	MST	(Default)
RLDRAM_ADDRESS14	MST	(Default)
RLDRAM_ADDRESS15	MST	(Default)
RLDRAM_ADDRESS16	MST	(Default)
RLDRAM_ADDRESS17	MST	(Default)
RLDRAM_ADDRESS18	MST	(Default)
RLDRAM_ADDRESS19	MST	(Default)
RLDRAM_ADDRESS20	MST	(Default)
RLDRAM_ADDRESS21	MST	(Default)
RLDRAM_ADDRESS22	MST	(Default)

Trace & Via Properties | Clearances | Nets | Parts | Constraint Templates

Net Topologies - Chained

Source Pins and Load Pins are kept together with an MST topology

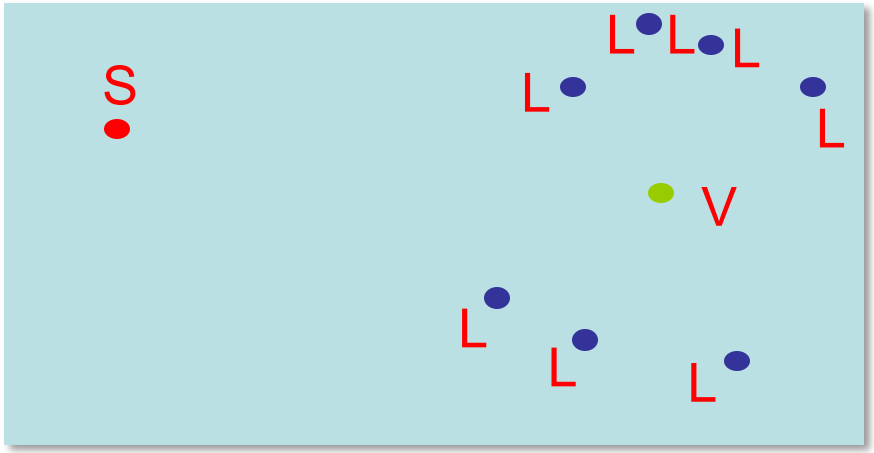


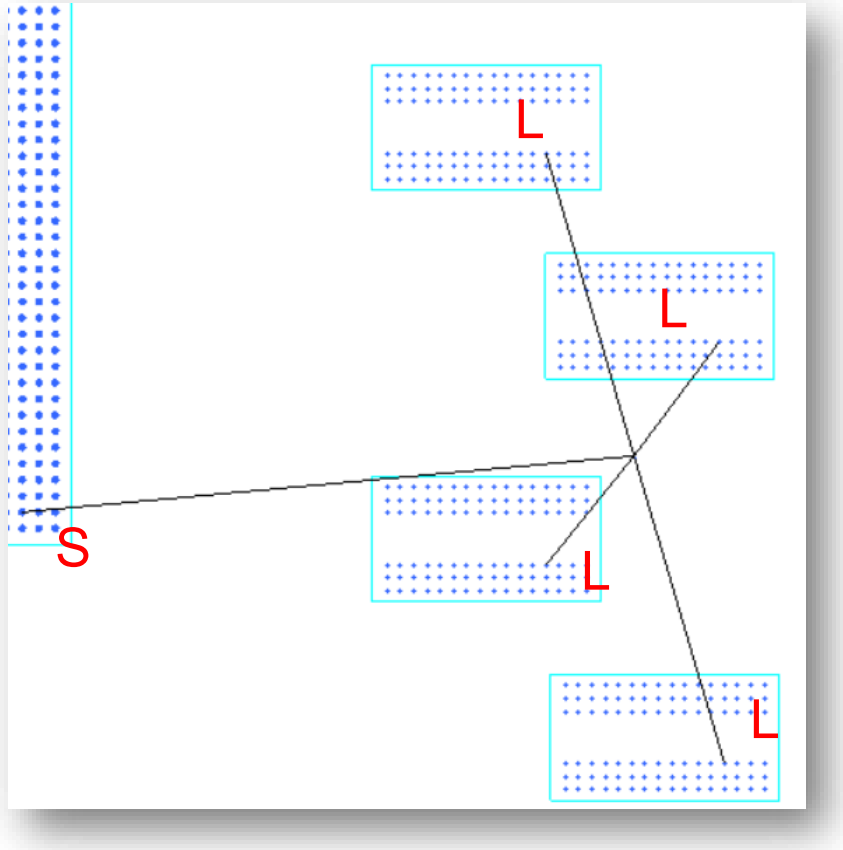


Net Topologies - Star

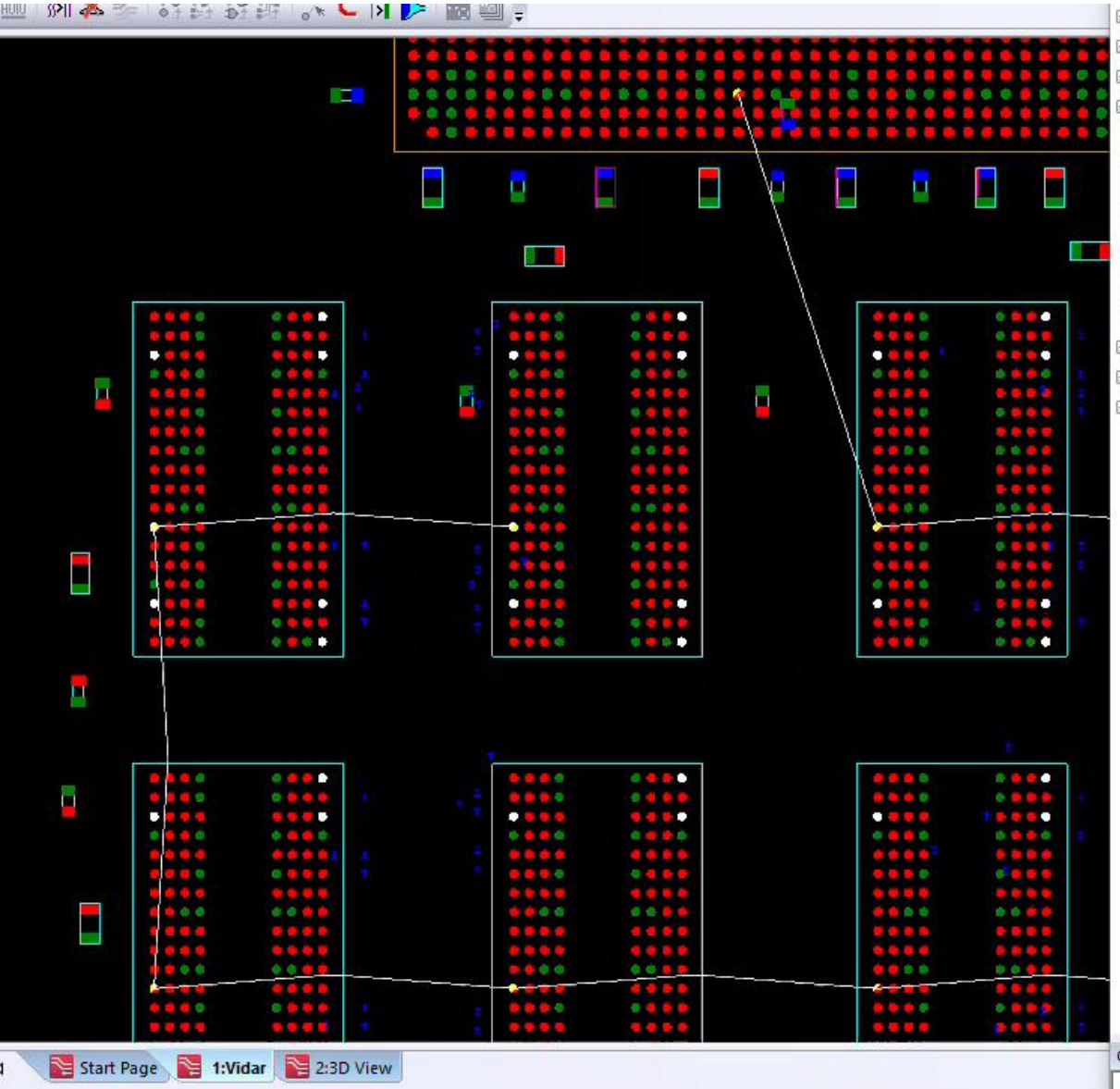
Star

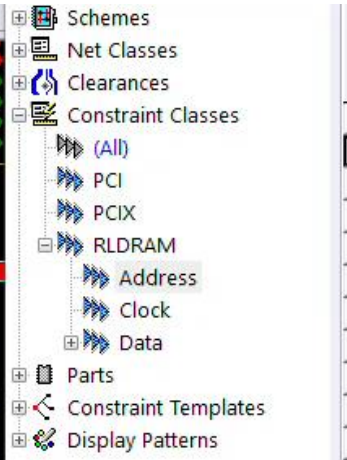
- From a single source to multiple loads using individual traces.
- Uses a single Virtual Pin placed at the mid point of the loads





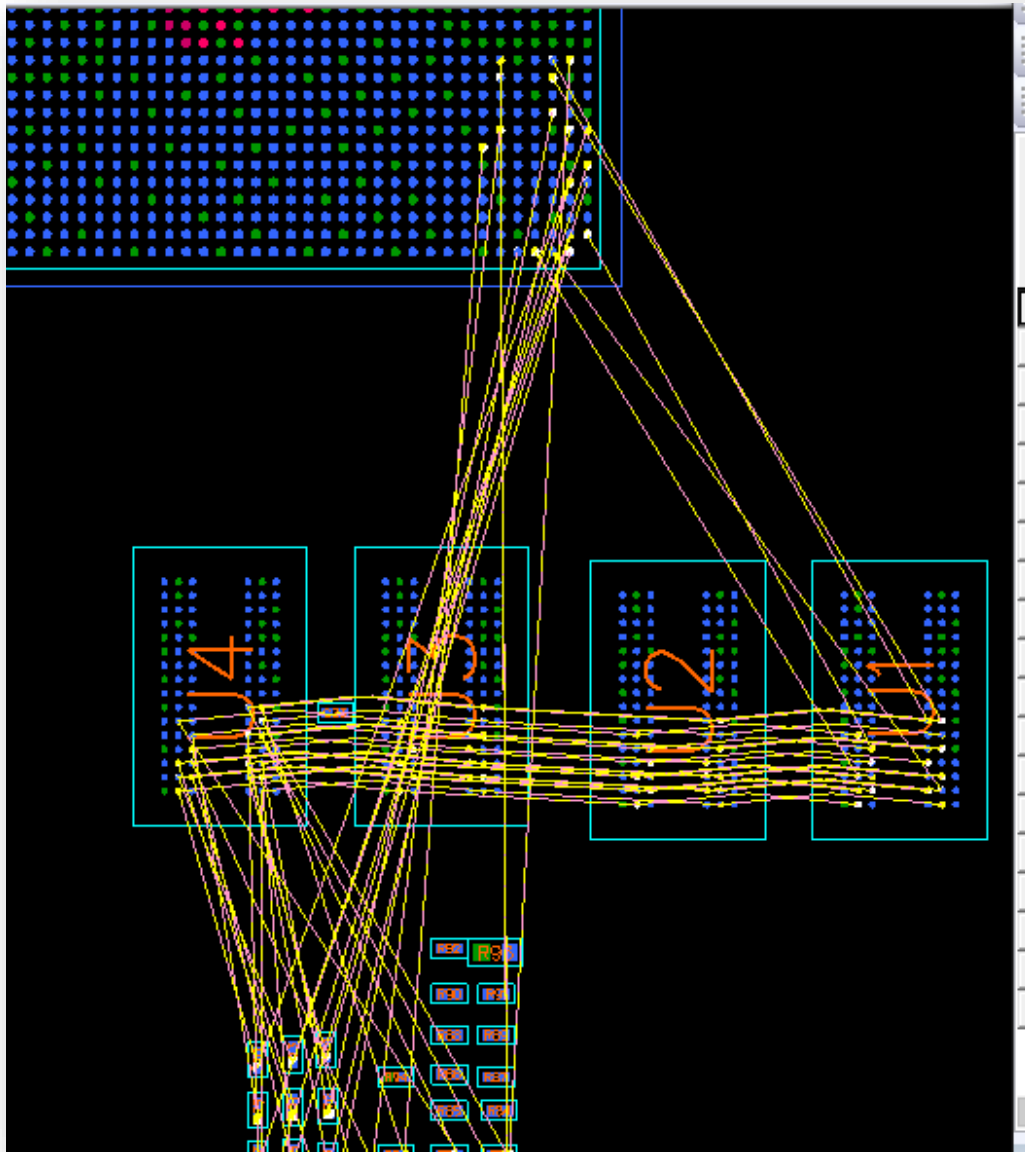
Star Topology Video





Constraint Class/Net	Topology Type	Net Class
Address	MST	(Default)
RLDRAM_ADDRESS0	MST	(Default)
RLDRAM_ADDRESS1	MST	(Default)
RLDRAM_ADDRESS2	MST	(Default)
RLDRAM_ADDRESS3	MST	(Default)
RLDRAM_ADDRESS4	MST	(Default)
RLDRAM_ADDRESS5	MST	(Default)
RLDRAM_ADDRESS6	MST	(Default)
RLDRAM_ADDRESS7	MST	(Default)
RLDRAM_ADDRESS8	MST	(Default)
RLDRAM_ADDRESS9	MST	(Default)
RLDRAM_ADDRESS10	MST	(Default)
RLDRAM_ADDRESS11	MST	(Default)
RLDRAM_ADDRESS12	MST	(Default)
RLDRAM_ADDRESS13	MST	(Default)
RLDRAM_ADDRESS14	MST	(Default)
RLDRAM_ADDRESS15	MST	(Default)
RLDRAM_ADDRESS16	MST	(Default)
RLDRAM_ADDRESS17	MST	(Default)
RLDRAM_ADDRESS18	MST	(Default)
RLDRAM_ADDRESS19	MST	(Default)
RLDRAM_ADDRESS20	MST	(Default)
RLDRAM_ADDRESS21	MST	(Default)
RLDRAM_ADDRESS22	MST	(Default)

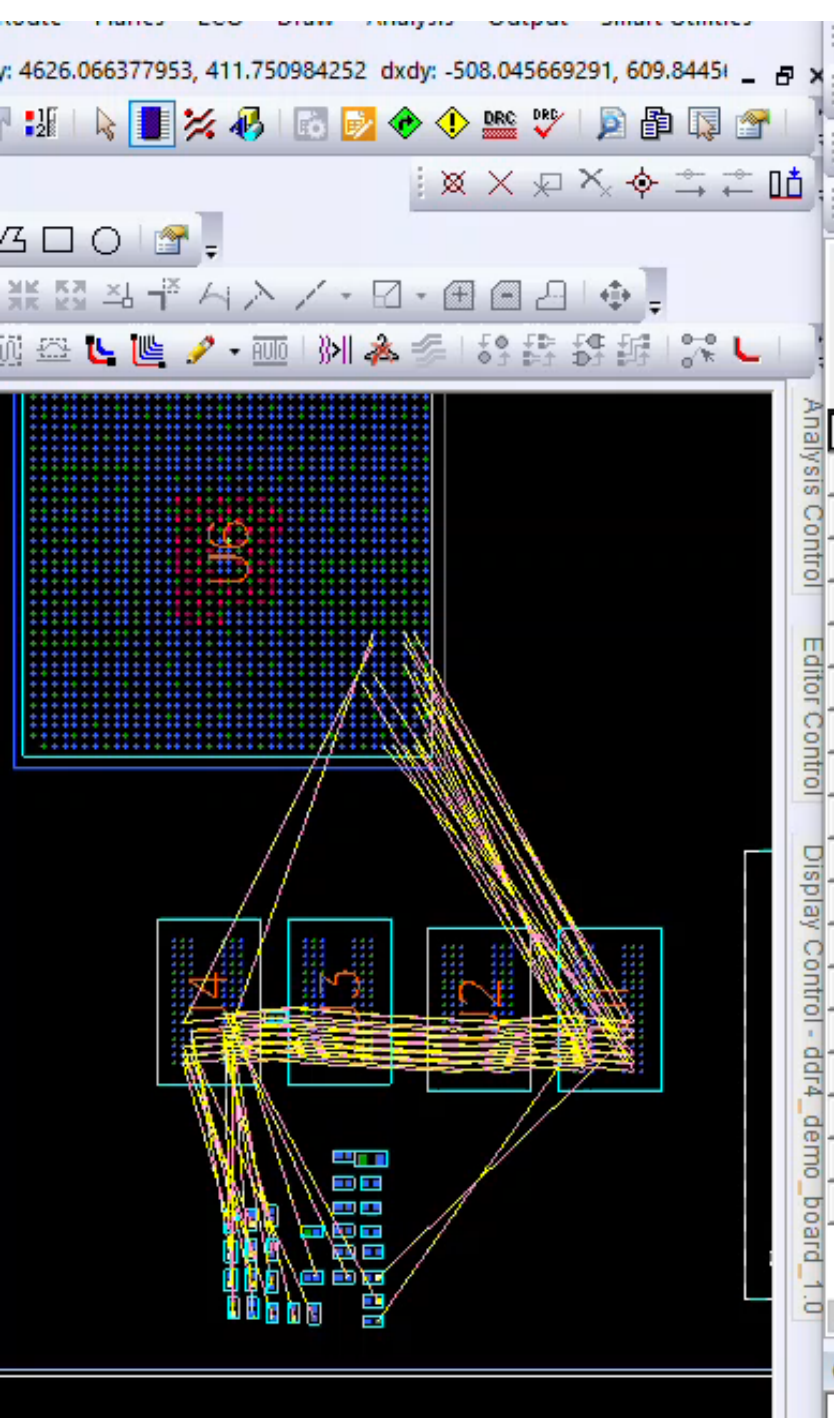
Custom Topology



Type here to search... | Enter phrase to find in help... | Enter script to execute...

Constraint Class/Net	Topology Type	Net Class	Di
DDR4_ADDR_CMD	Chained	(Default)	
DDR4_CK_N,DDR4_CK_P	Custom	(Default)	
PS_DDR_A0	Chained	(Default)	
PS_DDR_A1	Chained	(Default)	
PS_DDR_A2	Chained	(Default)	
PS_DDR_A3	Chained	(Default)	
PS_DDR_A4	Chained	(Default)	
PS_DDR_A5	Chained	(Default)	
PS_DDR_A6	Chained	(Default)	
PS_DDR_A7	Chained	(Default)	
PS_DDR_A8	Chained	(Default)	
PS_DDR_A9	Chained	(Default)	
PS_DDR_A10	Chained	(Default)	
PS_DDR_A11	Chained	(Default)	
PS_DDR_A12	Chained	(Default)	
PS_DDR_A13	Chained	(Default)	
PS_DDR_A14	Chained	(Default)	
PS_DDR_A15	Chained	(Default)	
PS_DDR_A16	Chained	(Default)	

Trace & Via Properties | Clearances | Nets | Parts | Constraint Templates



File Edit View Setup Filters Tools Data Output Help

Net Properties

Type here to search... Enter phrase to find in help... Enter script to execute...

Constraint Class/Net	Topology Type	Net Class	Display Pattern	# P
DDR4_ADDR_CMD	Chained	(Default)	(None)	
DDR4_CK_N,DDR4_CK_P	Custom	(Default)	(None)	
PS_DDR_A0	Chained	(Default)	(None)	
PS_DDR_A1	Chained	(Default)	(None)	
PS_DDR_A2	Chained	(Default)	(None)	
PS_DDR_A3	Chained	(Default)	(None)	
PS_DDR_A4	Chained	(Default)	(None)	
PS_DDR_A5	Chained	(Default)	(None)	
PS_DDR_A6	Chained	(Default)	(None)	
PS_DDR_A7	Chained	(Default)	(None)	
PS_DDR_A8	Chained	(Default)	(None)	
PS_DDR_A9	Chained	(Default)	(None)	
PS_DDR_A10	Chained	(Default)	(None)	
PS_DDR_A11	Chained	(Default)	(None)	
PS_DDR_A12	Chained	(Default)	(None)	
PS_DDR_A13	Chained	(Default)	(None)	
PS_DDR_A14	Chained	(Default)	(None)	
PS_DDR_A15	Chained	(Default)	(None)	
PS_DDR_A16	Chained	(Default)	(None)	

Trace & Via Properties | Clearances | Nets | Parts | Constraint Templates

Output

Analysis Control | Editor Control | Display Control - ddr4_demo_board_1.0

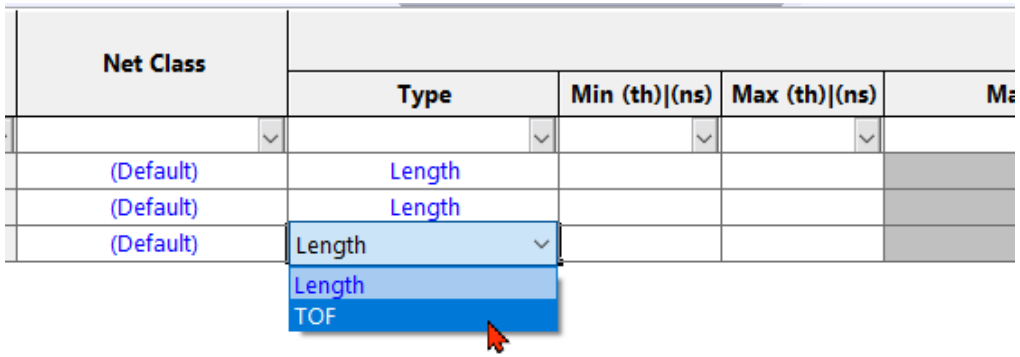
Constraining lengths

Via Lengths/Delays

The “Type” column in Constraint Manager in conjunction with the “Via Spans” Form in Xpedition (Setup Parameters) control how Via Lengths are calculated.

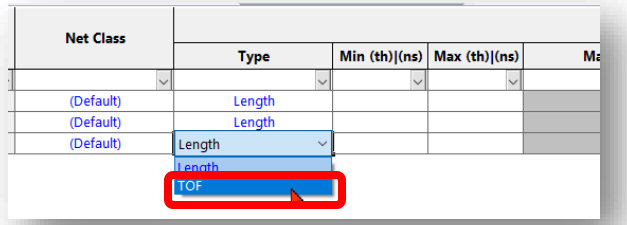
- Type = Length - Constraint Manager will use units of length (mm, um, etc)
- Type = TOF (Time of Flight) - Constraint Manager will use units of time (ns)

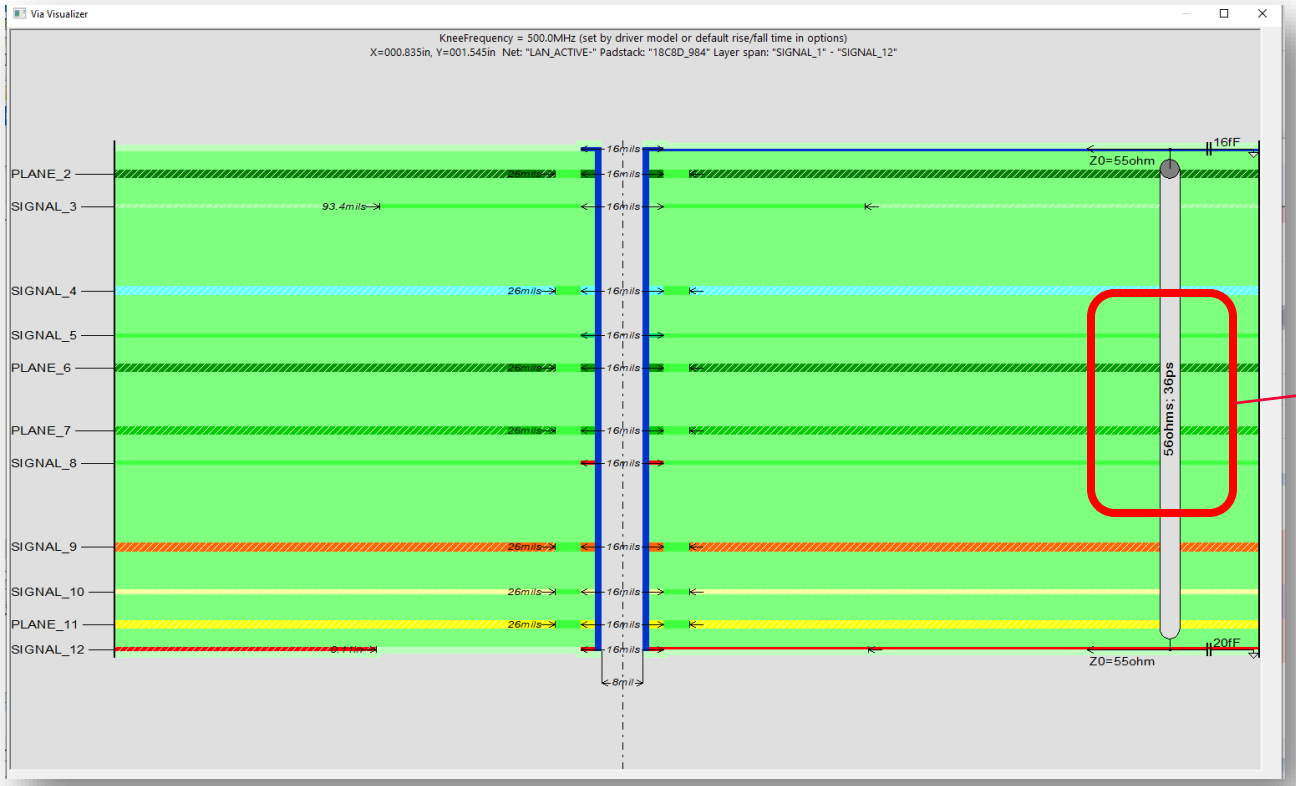
- When TOF / Via Delay is used, the *Via Delay* will be added for each via (in ns or ps)
- It is defined against the applicable Span in *Setup Parameters* > *Via Definitions*, pro-rated based on the proportion of the via span actually used by the signal - i.e., multiplied by the stackup thickness between the signal entry & exit layers (exclusive) divided by the span's start & end layers (exclusive).

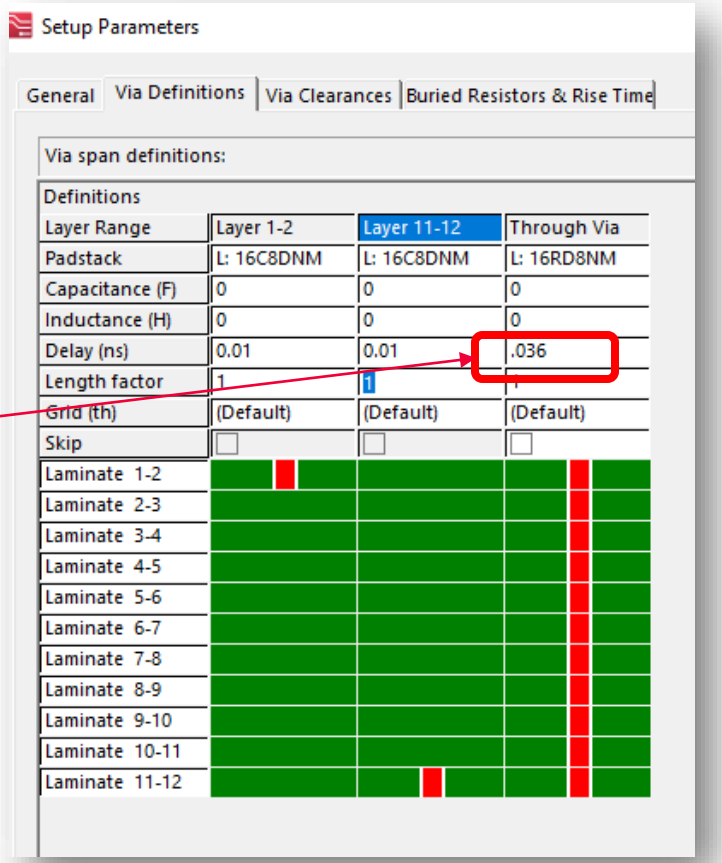


Vias TOF/Delay

- Use Hyperlynx to get the Via Delay (right click on a via that goes through all layers in BoardSim.)
- Enter the delay into the setup parameters/Via Definition form in Xpedition

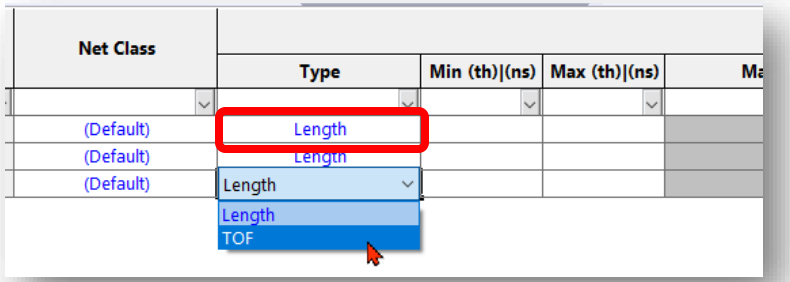


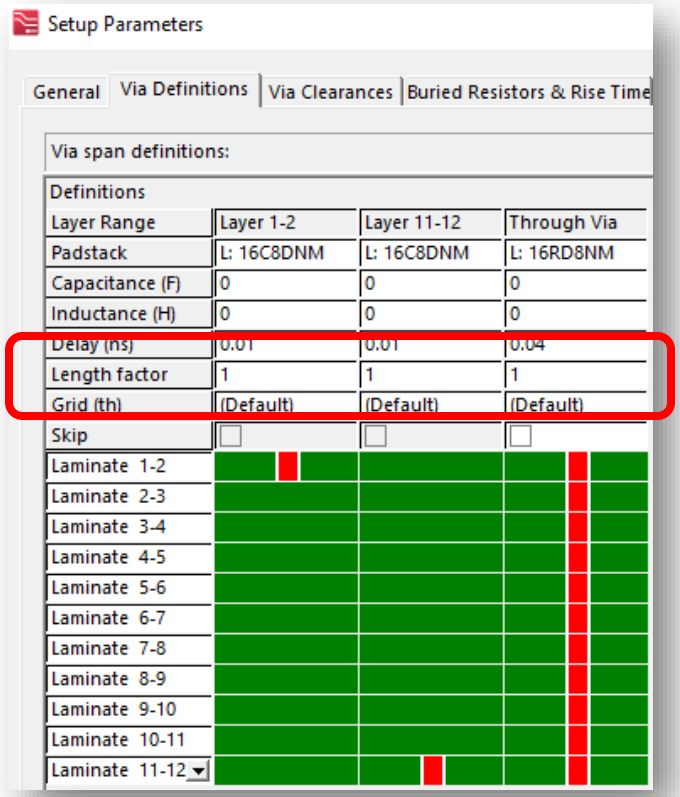




Vias Using Length Factor

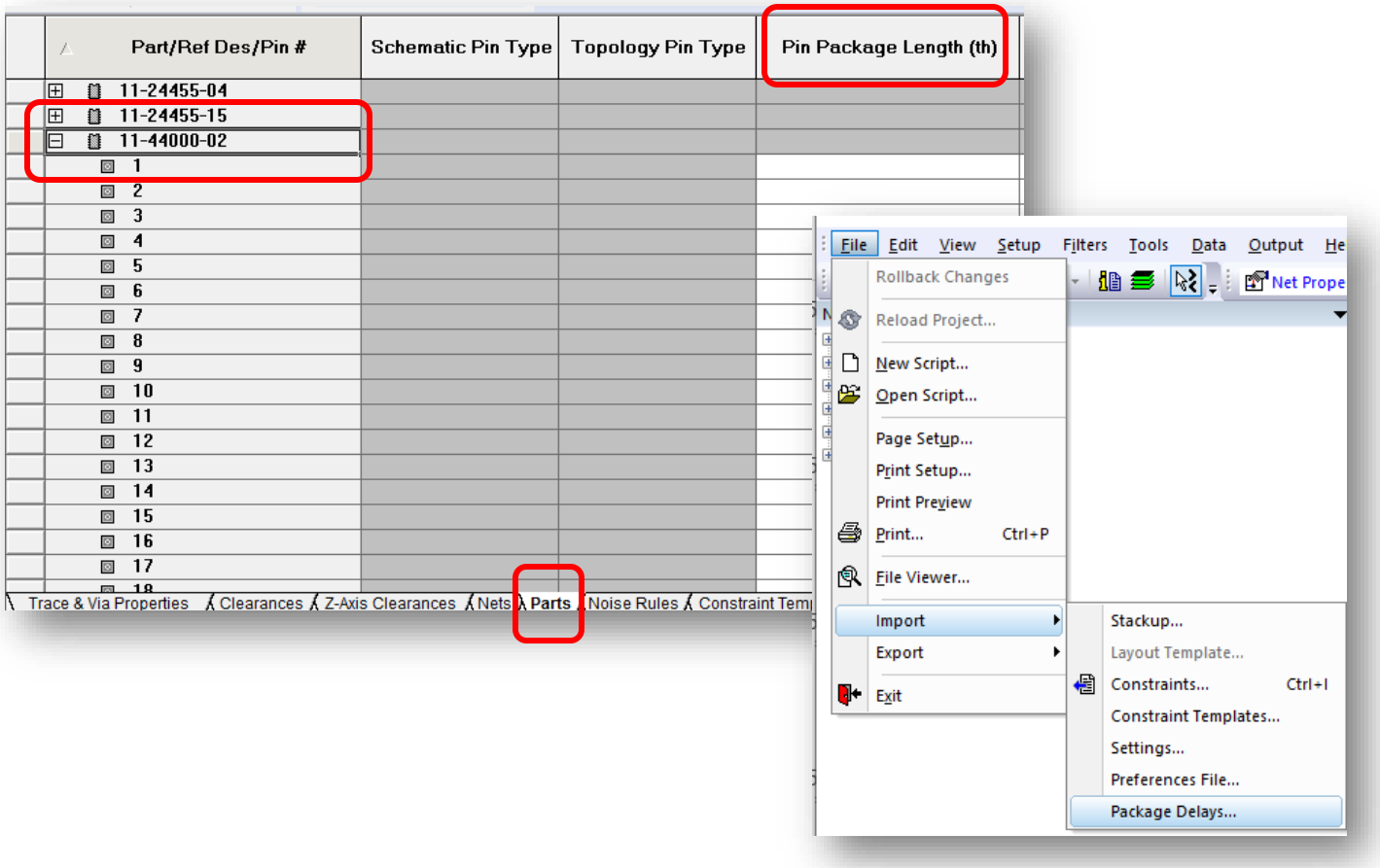
- If the “Type” Column in Constraint Manager is set to Length the System uses the Length Factor Section of the Via Definition form
- The length factor is a **multiplier**. The default is 0, which ignores the via barrel. If you want a net to include the Z distance when calculating the net length, you must define a length factor > 0.
- You can set up each span independently. If you want all via spans to be used in the net length calculation, then each span must have a factor defined.
- The length calculated is based on the layer stackup as well as on where the traces start and end.

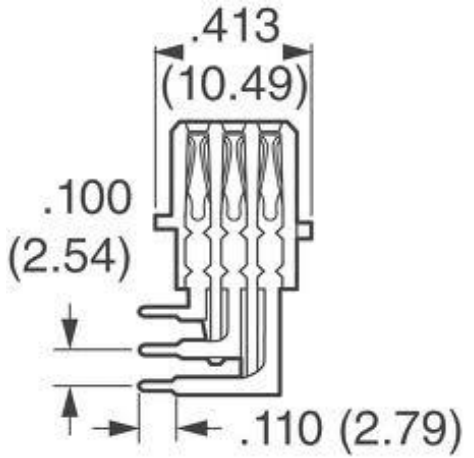


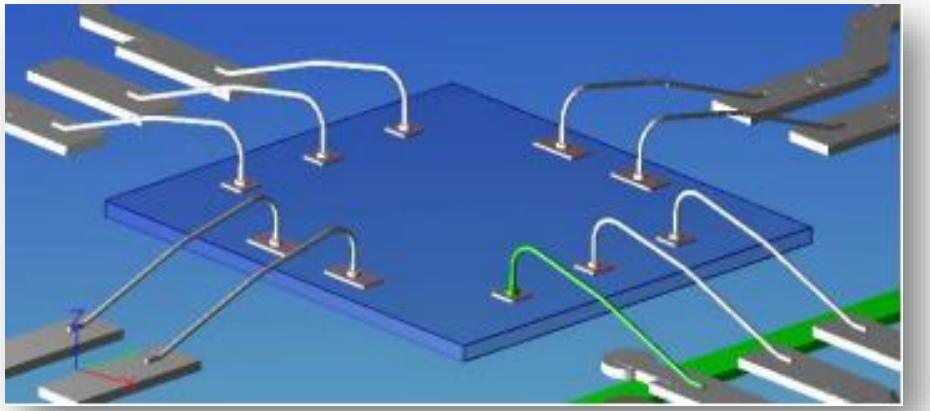


Package Pin Lengths

- You can compensate for extra lengths in IC or Connectors in Parts – Pin Package Length
- Can be imported from a file (file format in documentation)







What are Pin Pairs?

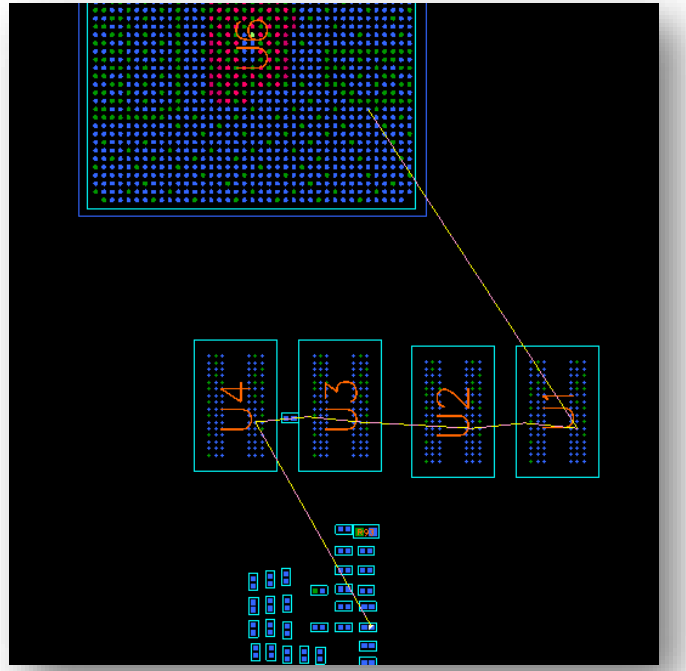
- Pin Pairs are literally a pair of pins on a net.
- Any 2 pins on the net can be a pin pair.
- You can set a delay rule from any pin to any other pin.

Example: an Address line is routed between from Controller to 4 memory devices

- It is required to match the length between each chip, and the entire length can not be more than7 inches.

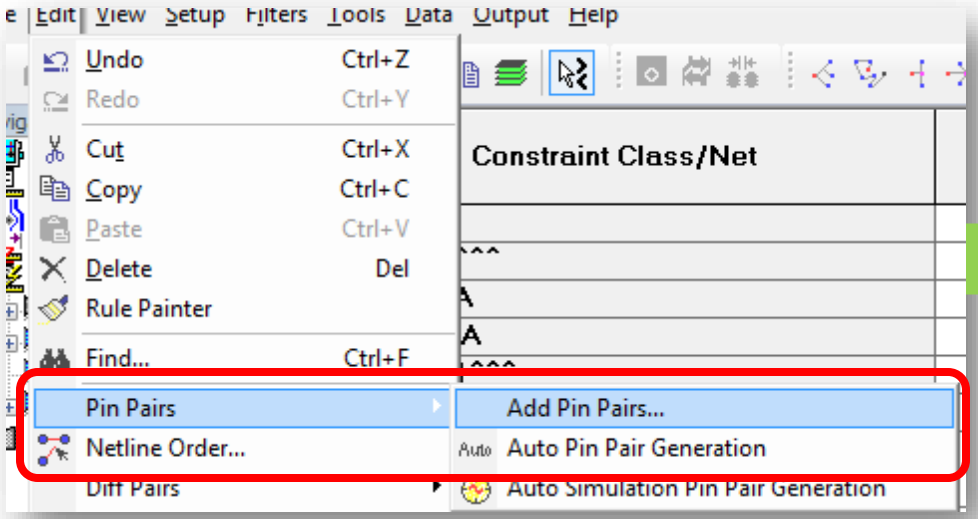
Possible Pin Pairs:

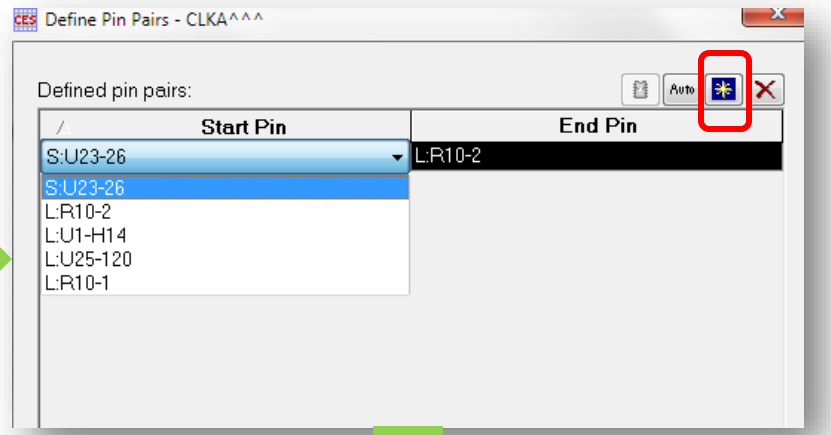
U6-U1 U1-U2 U6-U4 U1-U3 U4-R9

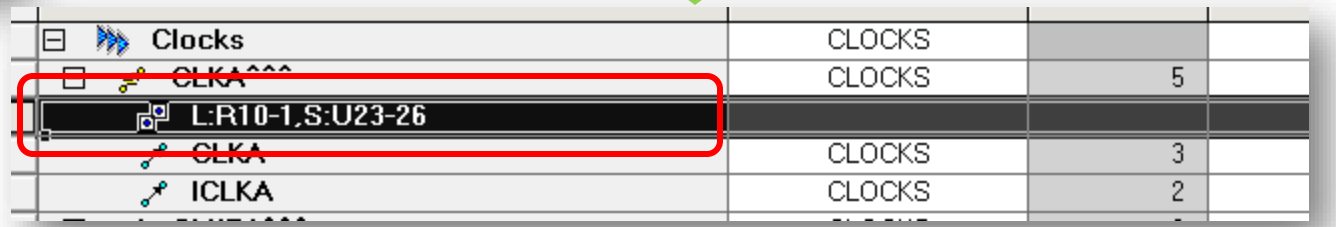


Creating a Pin Pair

- Select a net
- Set the net topology to be “Custom”
- Select Edit→“Add Pin Pairs”
- Use the Blue Asterisk to add new rows of pin pairs.
- The Pin Pair then becomes available in the main CES window under the net to which it belongs.

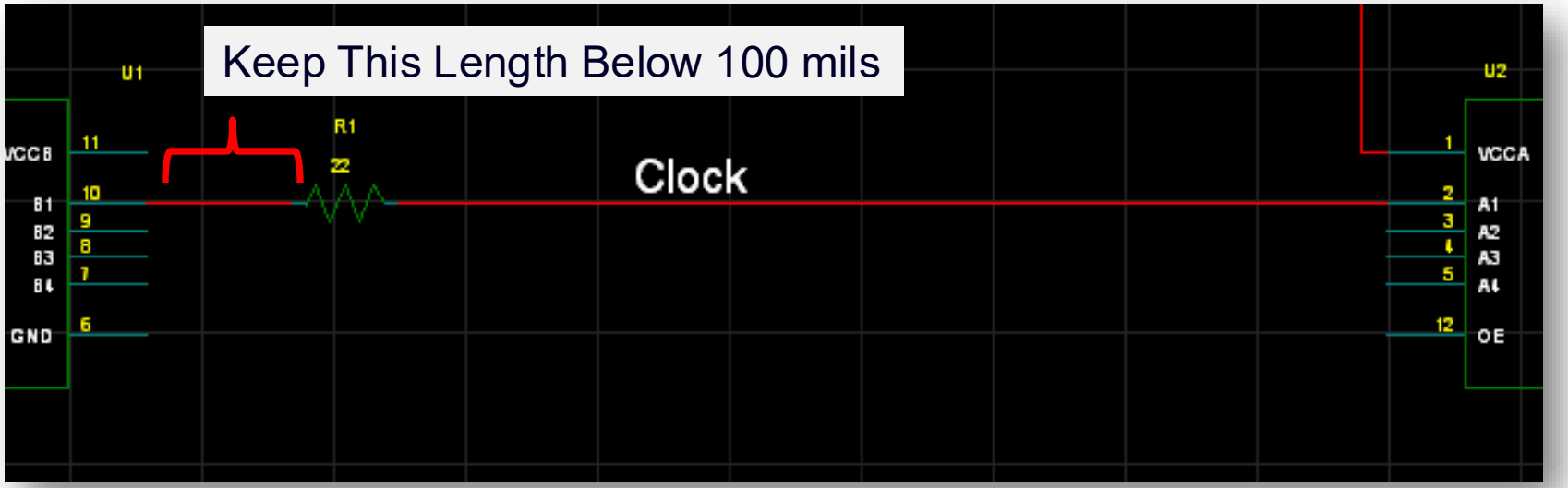


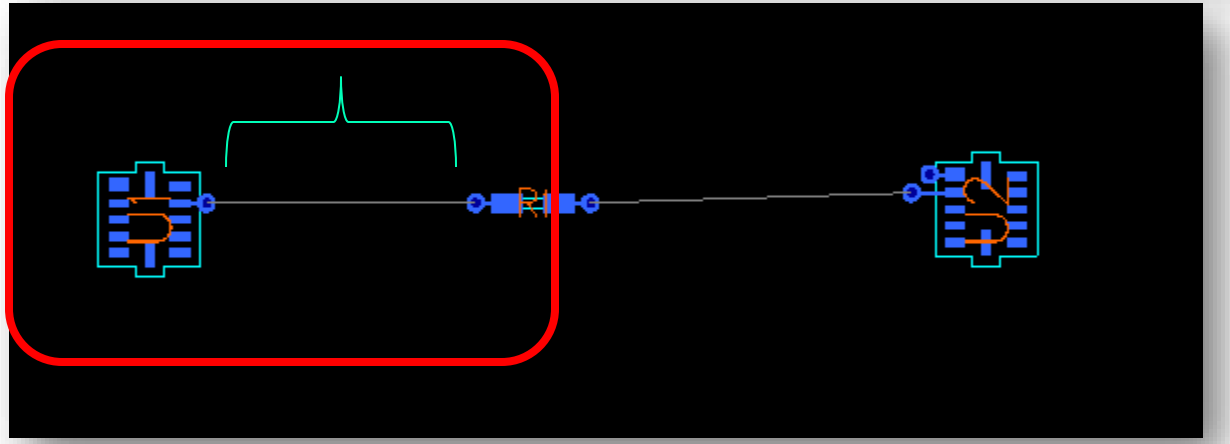




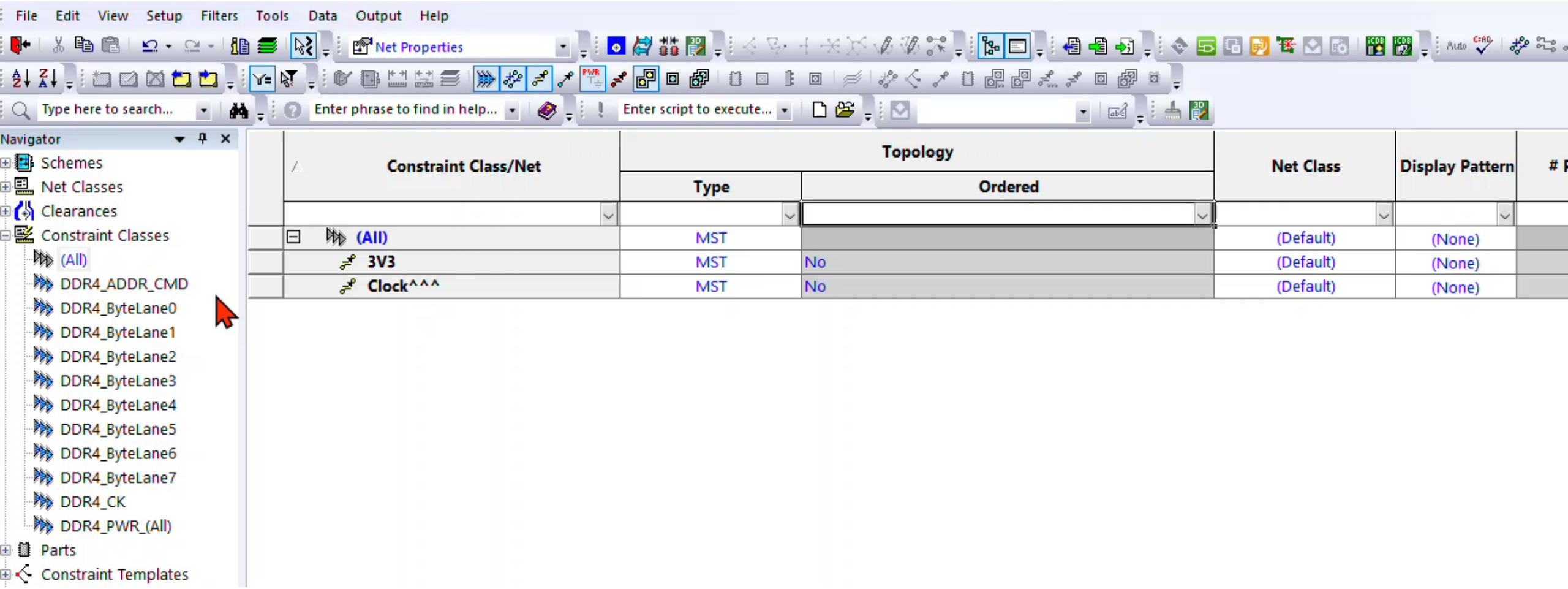
Using a pin pair and a Max Length Rule.

Use the Constraint Manager to ensure that R1 is placed close to U2





Create the Pin Pair

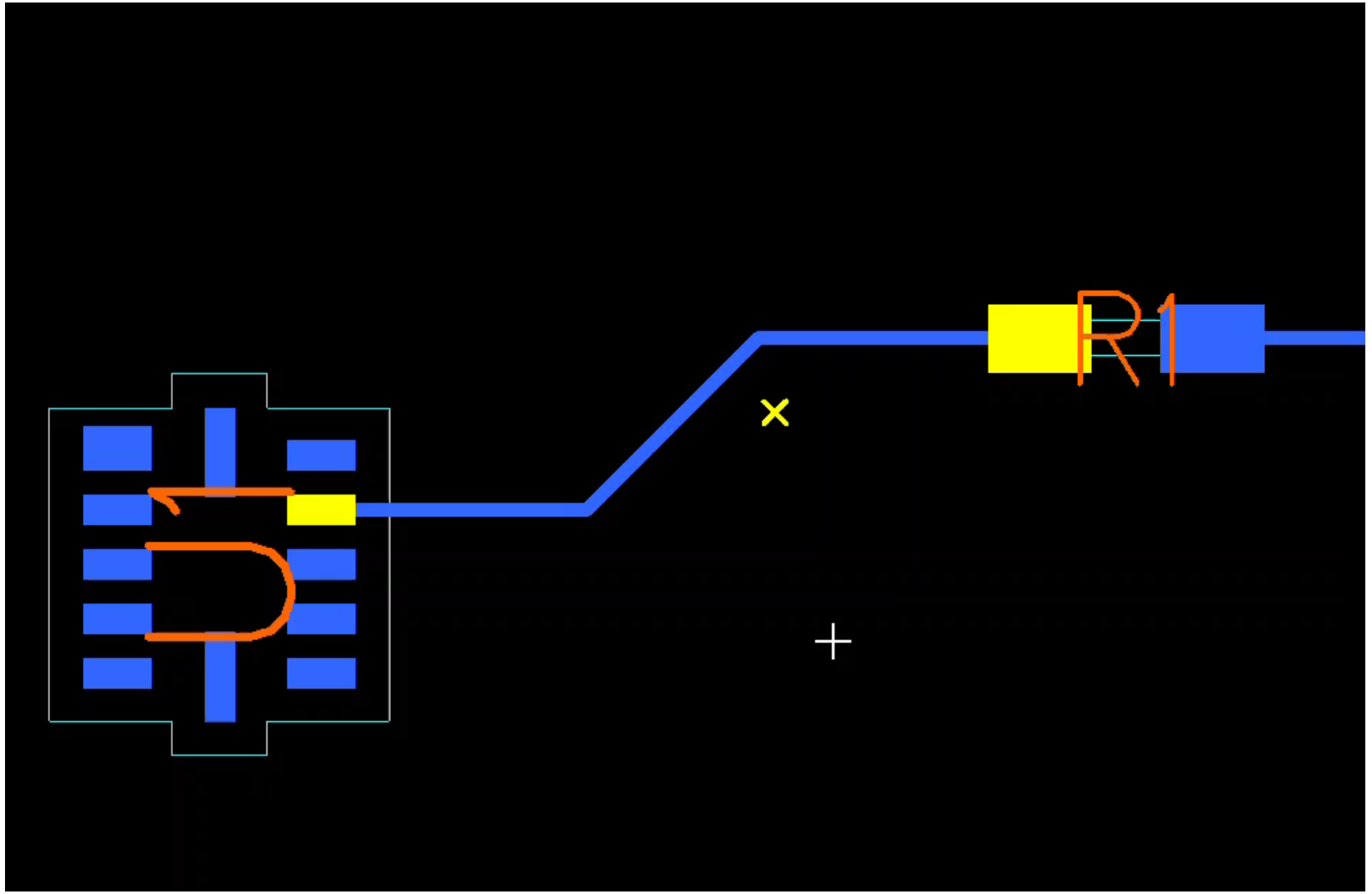


Set the Max Length Rule on the pin pair

Constraint Class/Net	Min (th)|(ns)	Max (th)|(ns)	Actual (th)|(ns)	Manhattan	Min Length (th)
(All)					
3V3					
Clock^^^					
S:U1-10,L:R1-1					

	Min (th)|(ns)	Max (th)|(ns)	Actual (th)|(ns)	Manhattan
(All)				
3V3			25.563	0
Clock^^^			706.326	708.945
S:U1-10,L:R1-1		100	70.242	70.661

Problem Solved



Length Constraints

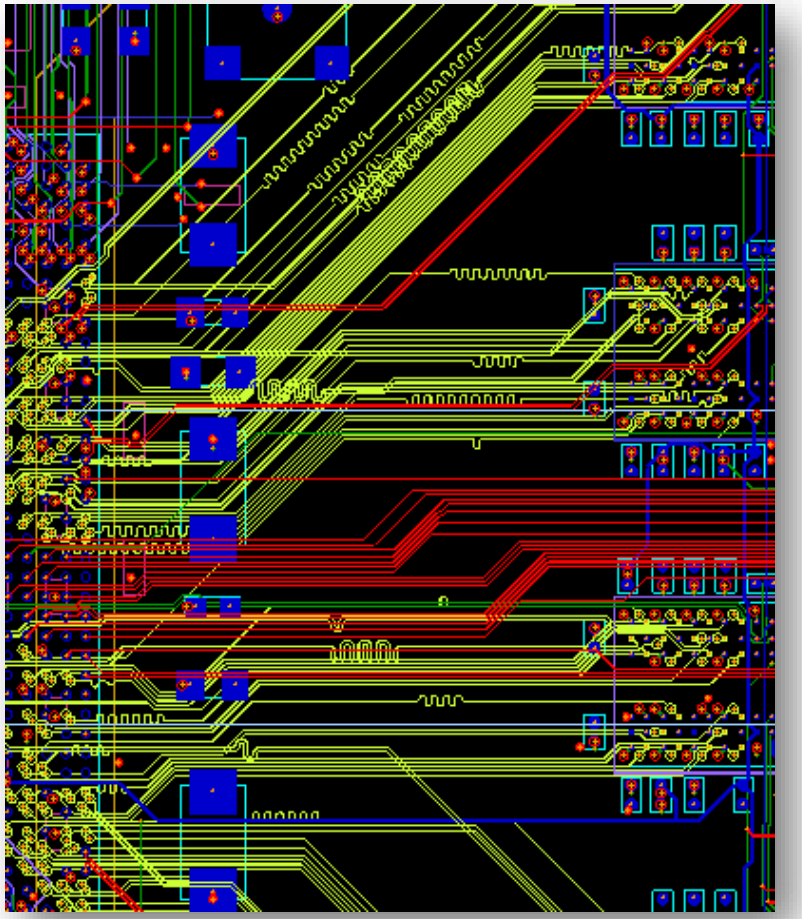
- Length can be constrained on an entire net
- Between any two pins on a net (called a pin pair)
- Lengths can be constrained in 3 main categories:
  - **Min/Max Length** – Specify the Min and Max Length for a net or pin pair
  - **Matched Length** – Specify a group of nets or pin pairs need to have the same length ± tol
  - **Delay Formulas** – Specify the length of pin pair is the function of another pin pair

Matched Lengths

Example: Match the length of the data lines so they are all within 100 mils of each other.

The tolerance of 100 mils means +/-50th

Constraint Class/Net	Net Class	Length or TOF Delay							
		Type	Min (th)|(ns)	Max (th)|(ns)	Actual	Manha	Min Length	Match	Tol (th)|(ns)
⊞ DDR2_CONTROL	DDR2_Addr_Cntrl	Length							
⊟ DDR2_DATA	DDR2_Data	Length							
⊟ GROUP_0	DDR2_Data	Length							
⊞ DDR2_DATA[0]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[1]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[2]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[3]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[4]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[5]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[6]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[7]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[8]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[9]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[10]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[11]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[12]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[13]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[14]	DDR2_Data	Length						ML2	100.000
⊞ DDR2_DATA[15]	DDR2_Data	Length						ML2	100.000



Data Lines After Tuning in Xpedition

Clearances

Clearances Example

A Design contains 3 classes of nets (Net Classes)

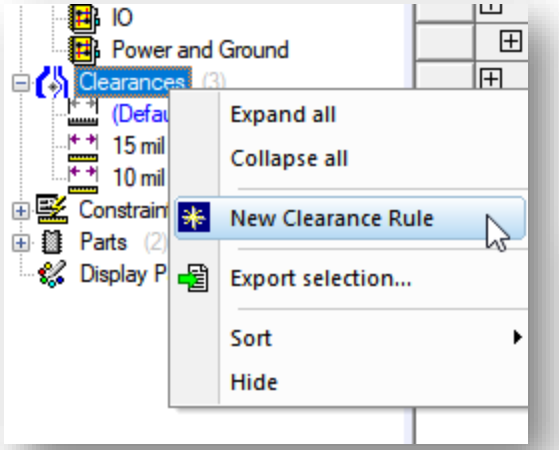
- Default Class
- Clocks Class
- High Speed Links (SerDes) Class

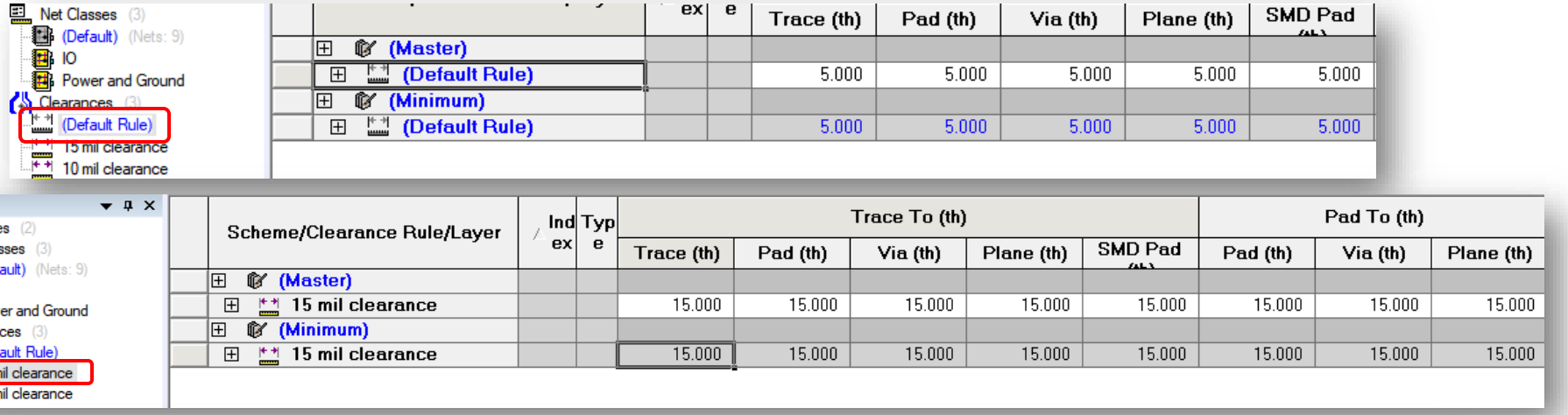
Requirements

- Keep Clocks **15 mils** from every other class
- High Speed Links can be routed **10 mils** from each other, but kept 15 mils away from everything else
- Default Class nets can be routed with **5 mil** lines and spacing

Clearances

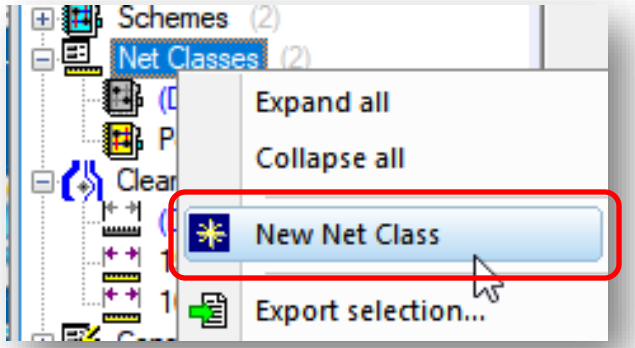
- We will need 3 sets of clearance rules – Default will handle 5 Mil clearances, and then 10 mil and 15 mil will handle the other clearances.
- Setup the clearance for each rule.
- **Note**: the rule has not been applied to any nets.

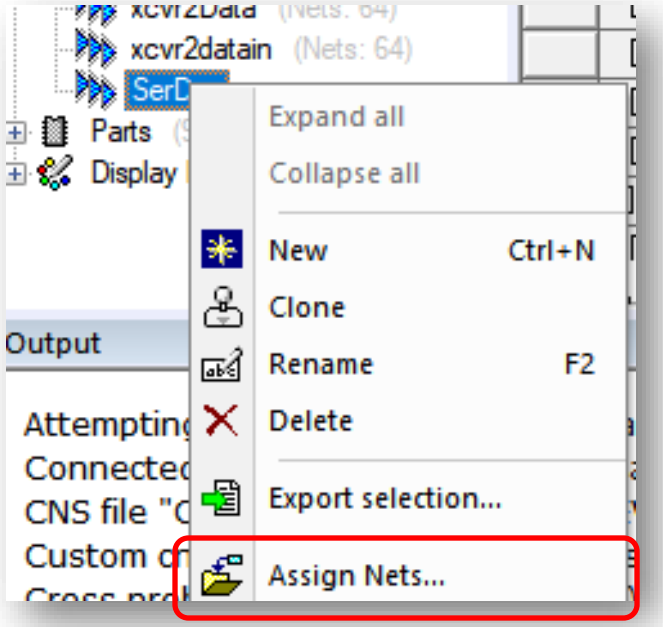


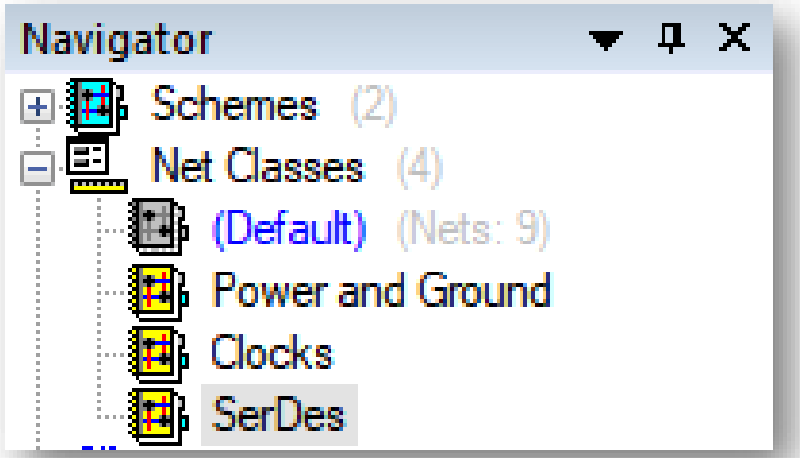


Create the Net Classes

- Right Click on Net Classes to create a new class
- Right Click on a Net Class to assign nets to it

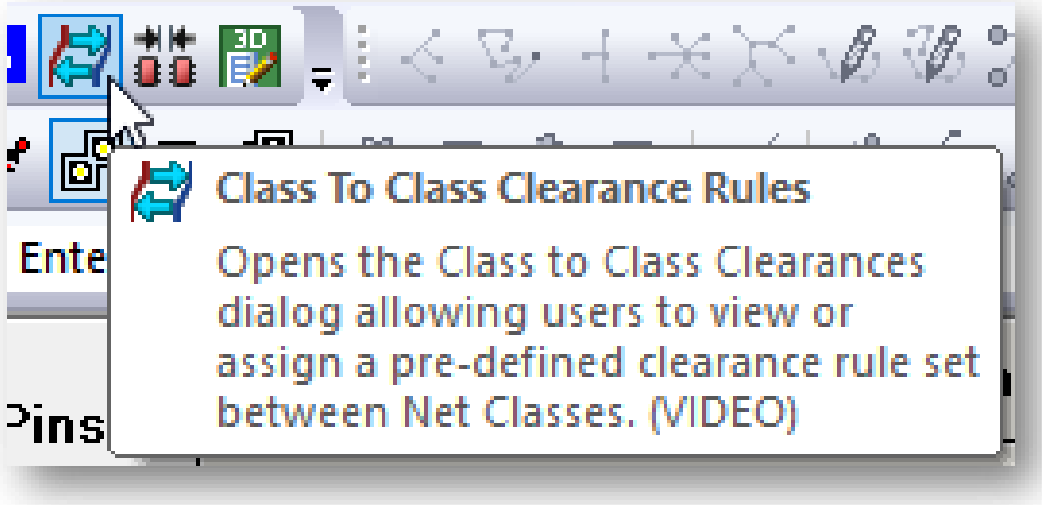


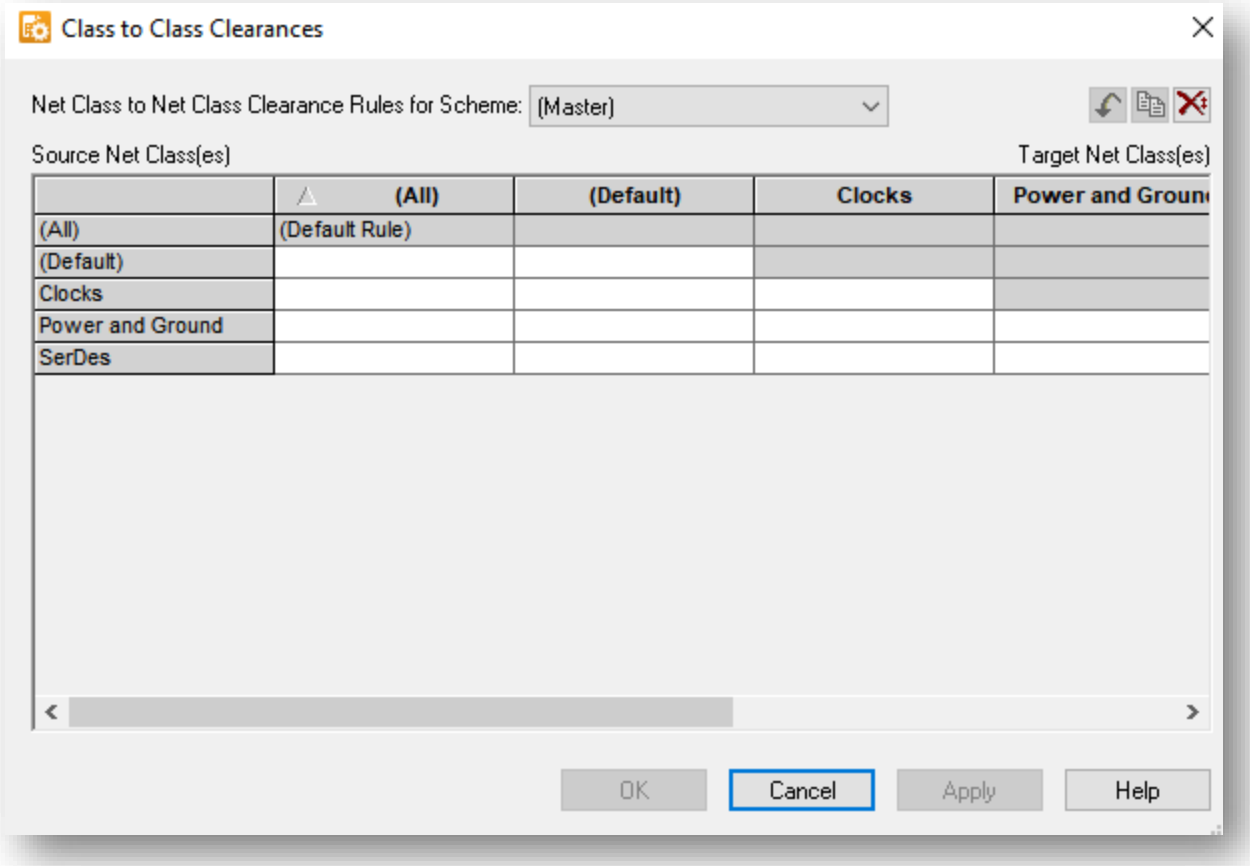




Class to Class Dialog

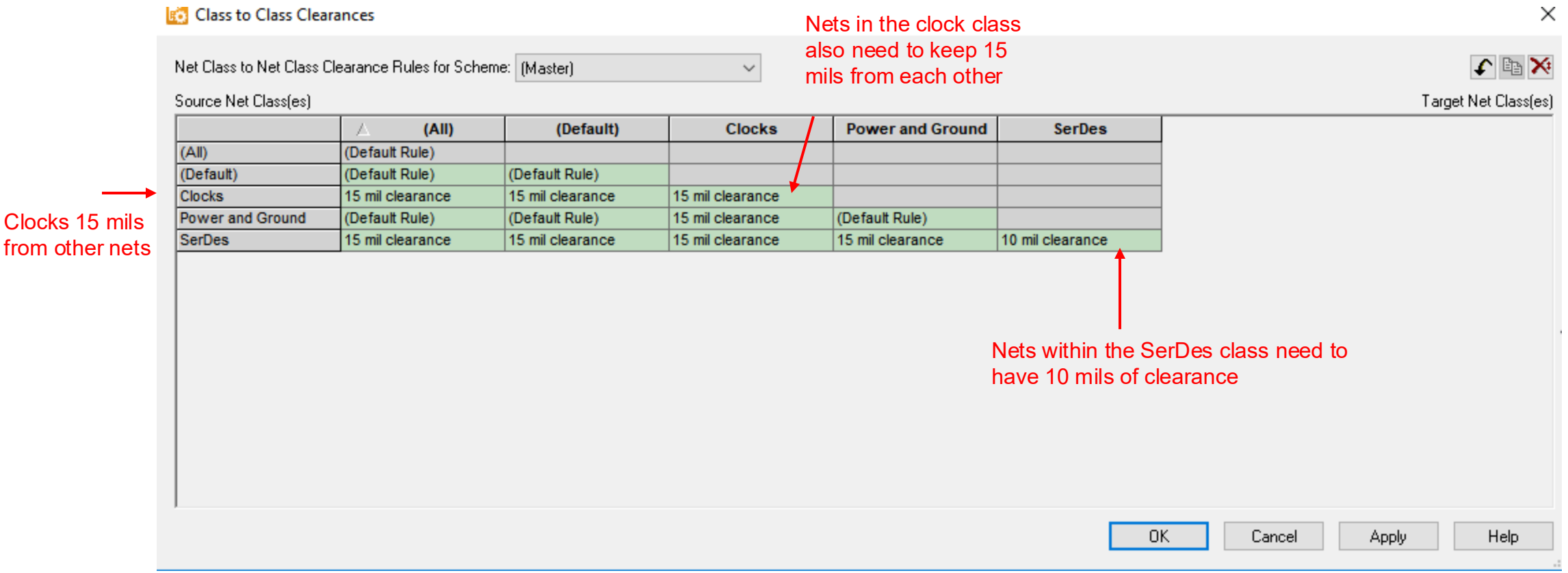
- Click on “Class to Class Clearance Rules”
- Any Blank Cell will use the default Rule





Class to Class Dialog

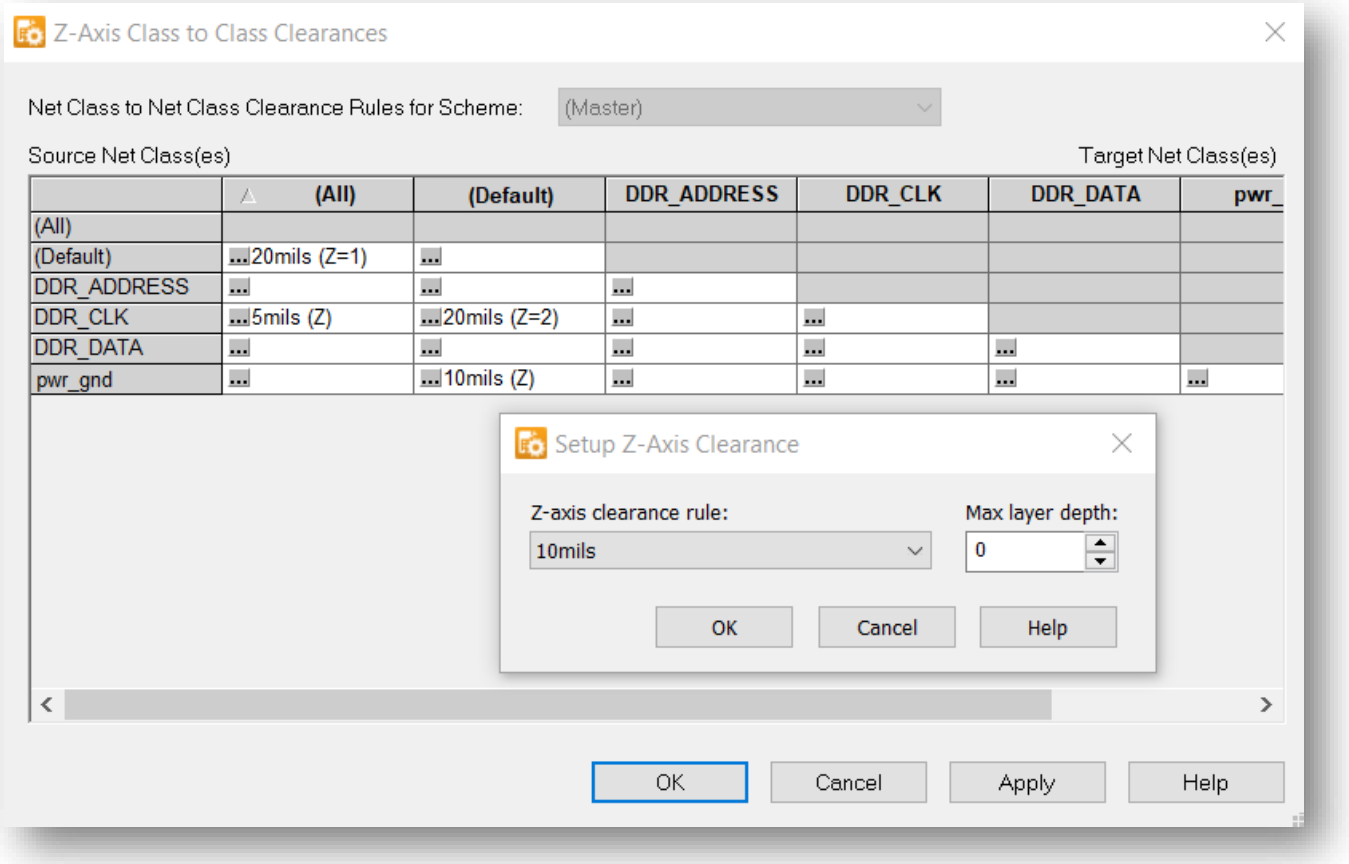
- Fill in the various cells to setup rules from one class to another
- Setup the clearance within a class where a horizontal and vertical column coincide for the same class.



	(All)	(Default)	Clocks	Power and Ground	SerDes
(All)	(Default Rule)				
(Default)	(Default Rule)	(Default Rule)			
Clocks	15 mil clearance	15 mil clearance	15 mil clearance		
Power and Ground	(Default Rule)	(Default Rule)	15 mil clearance	(Default Rule)	
SerDes	15 mil clearance	15 mil clearance	15 mil clearance	15 mil clearance	10 mil clearance

Z-Axis Clearance Manager

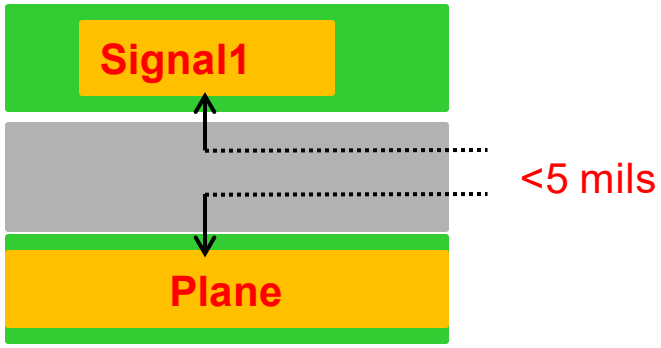
- Controls clearance rules on adjacent layers
- The Layer Depth can be set from the ‘Z Axis Class to Class Clearances’ dialog



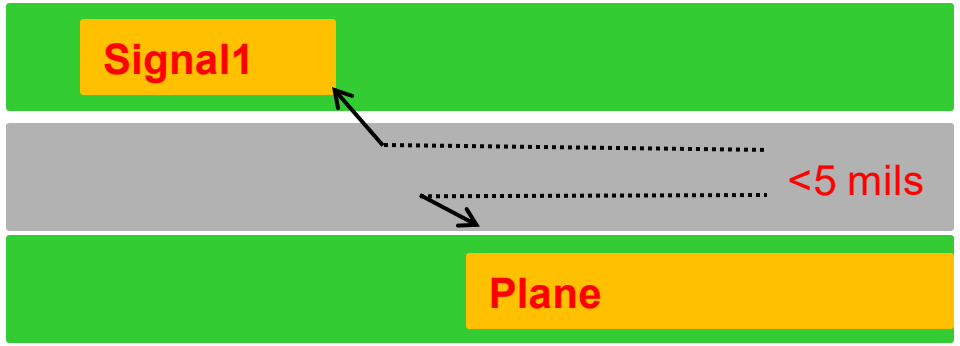
Z Axis Clearance Control

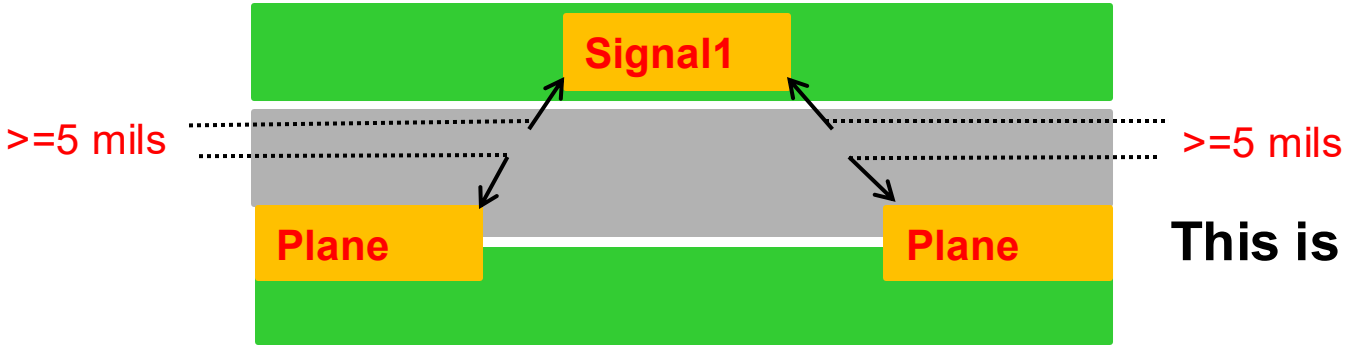
How Z Axis Clearances Work:
Note: You can substitute “Plane” with Signal from another class.
i.e., High Voltage to Low Voltage

Rule Violation!



Rule Violation!

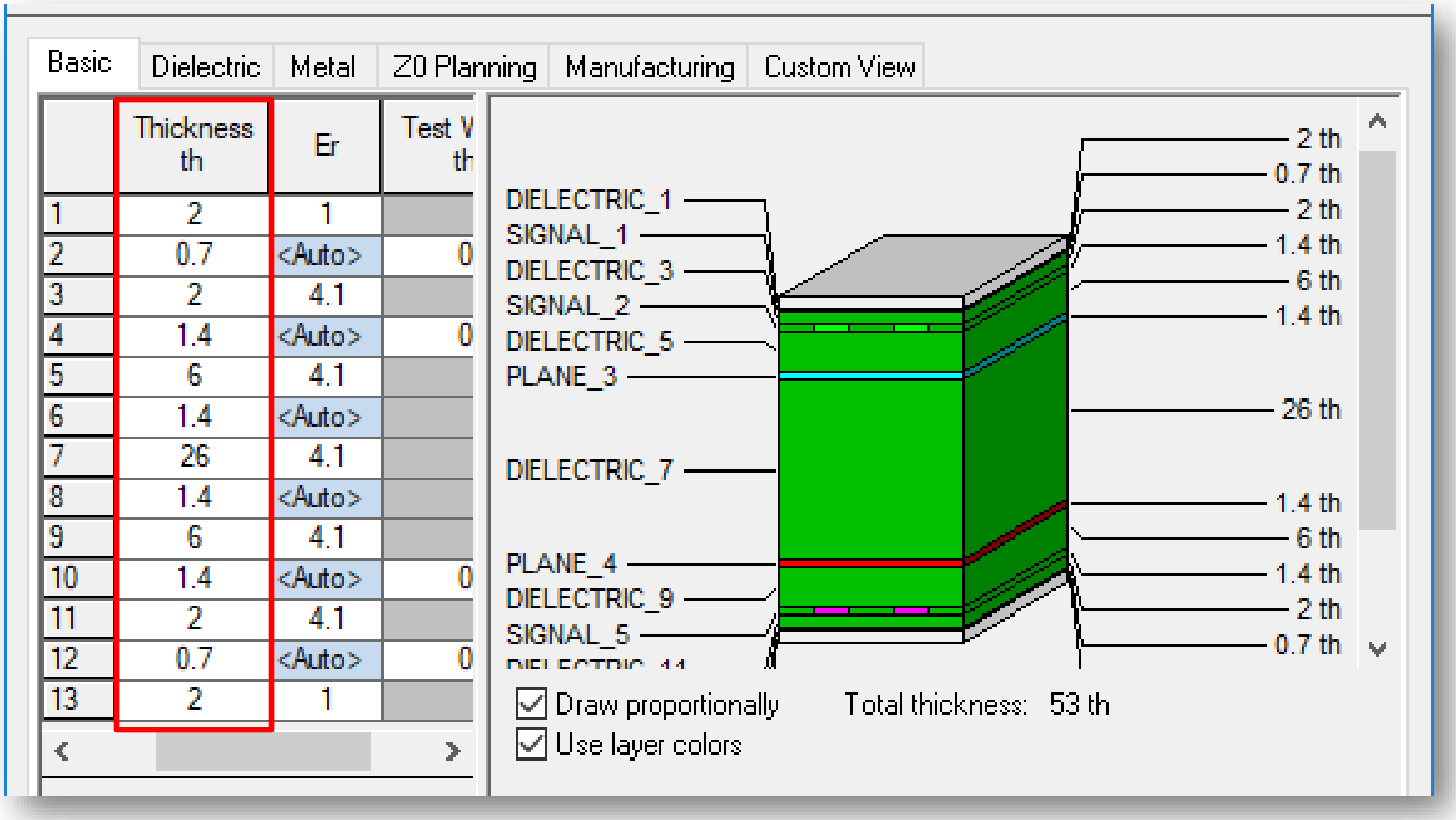




This is okay!

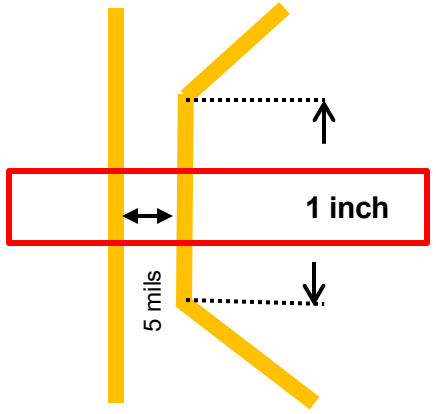
Z Axis and the Stackup

For Z-Axis rules, you must fill in the correct dimensions in “Thickness’’ Column for the layer stackup.

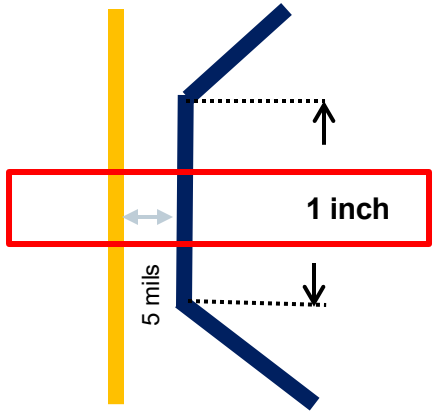


What are Parallelism rules?

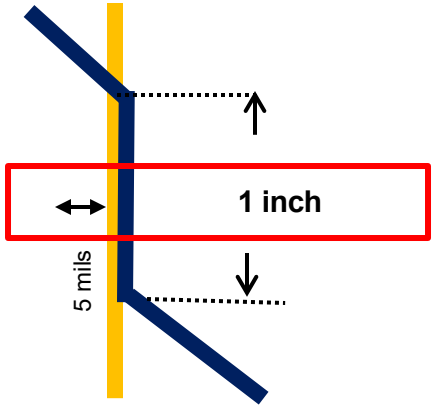
- Parallelism rules control the distance that specified nets can be routed parallel to each other
- They are used to reduce the chance of crosstalk.
- A parallelism rule consists of two parameters: Length and Distance.
- Parallelism rules can be defined for the same and adjacent layers.
- A net or class can have multiple parallelism rules.
- HyperLynx should always be used to verify crosstalk levels are low enough.



Rule: These traces on the same layer are not allowed to be 5 mils apart for more than an inch.

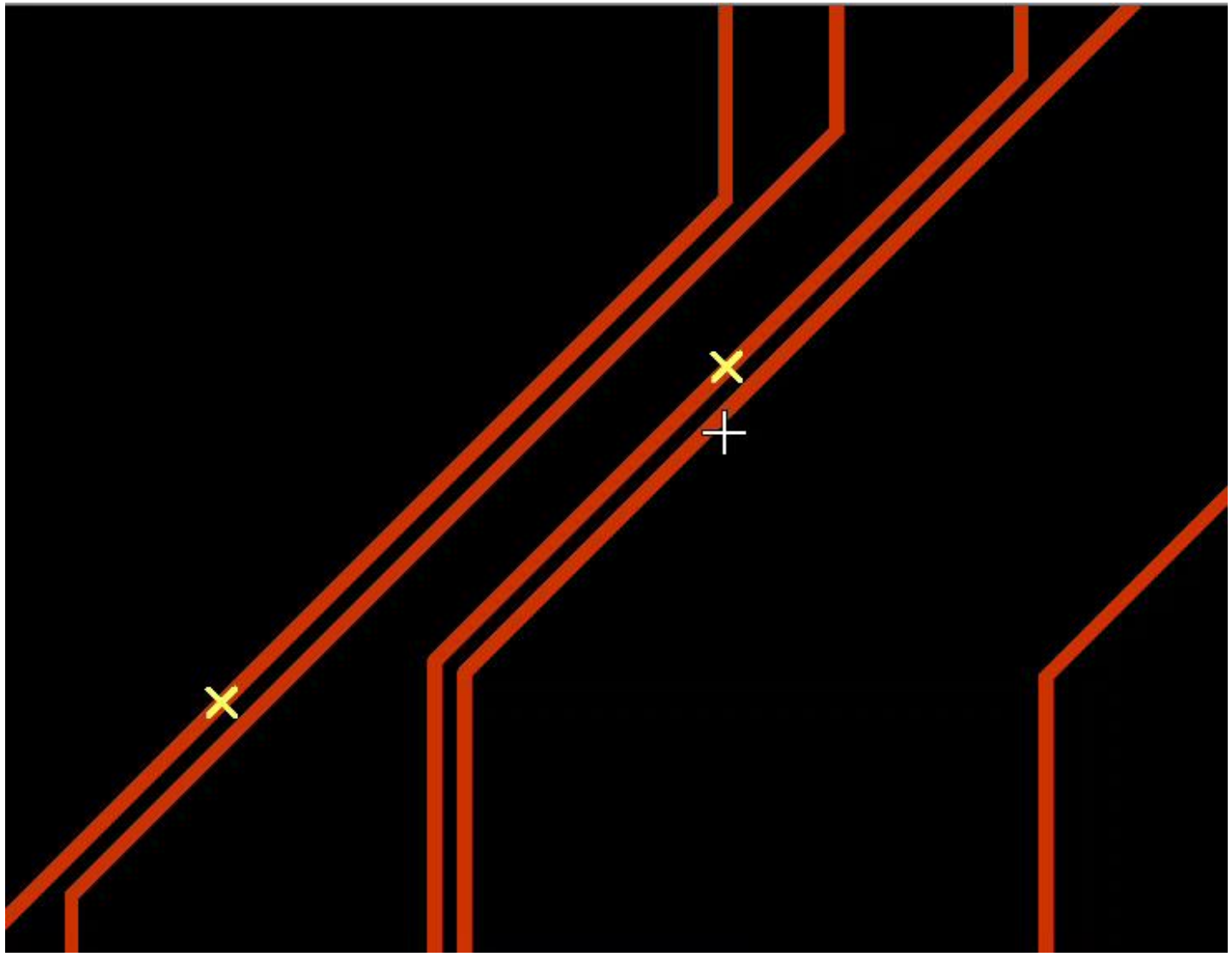


Rule: These traces on adjacent layers are not allowed to be 5 mils apart for more than an inch.

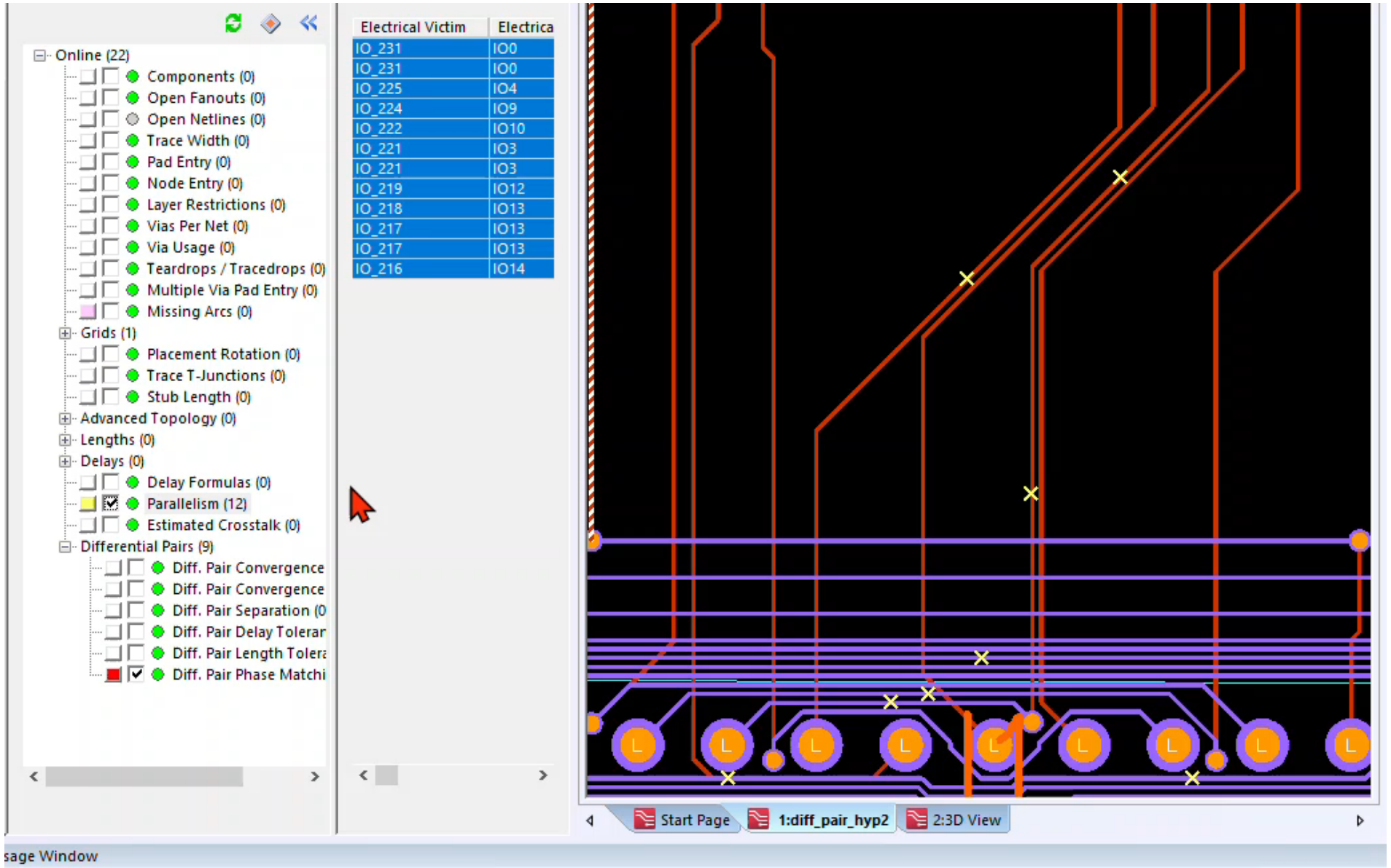


Rule: These traces on adjacent layers are not allowed to be 5 mils apart for more than an inch.

Fixing Parallelism – Manual Method



Fixing Parallelism – Using Spacers

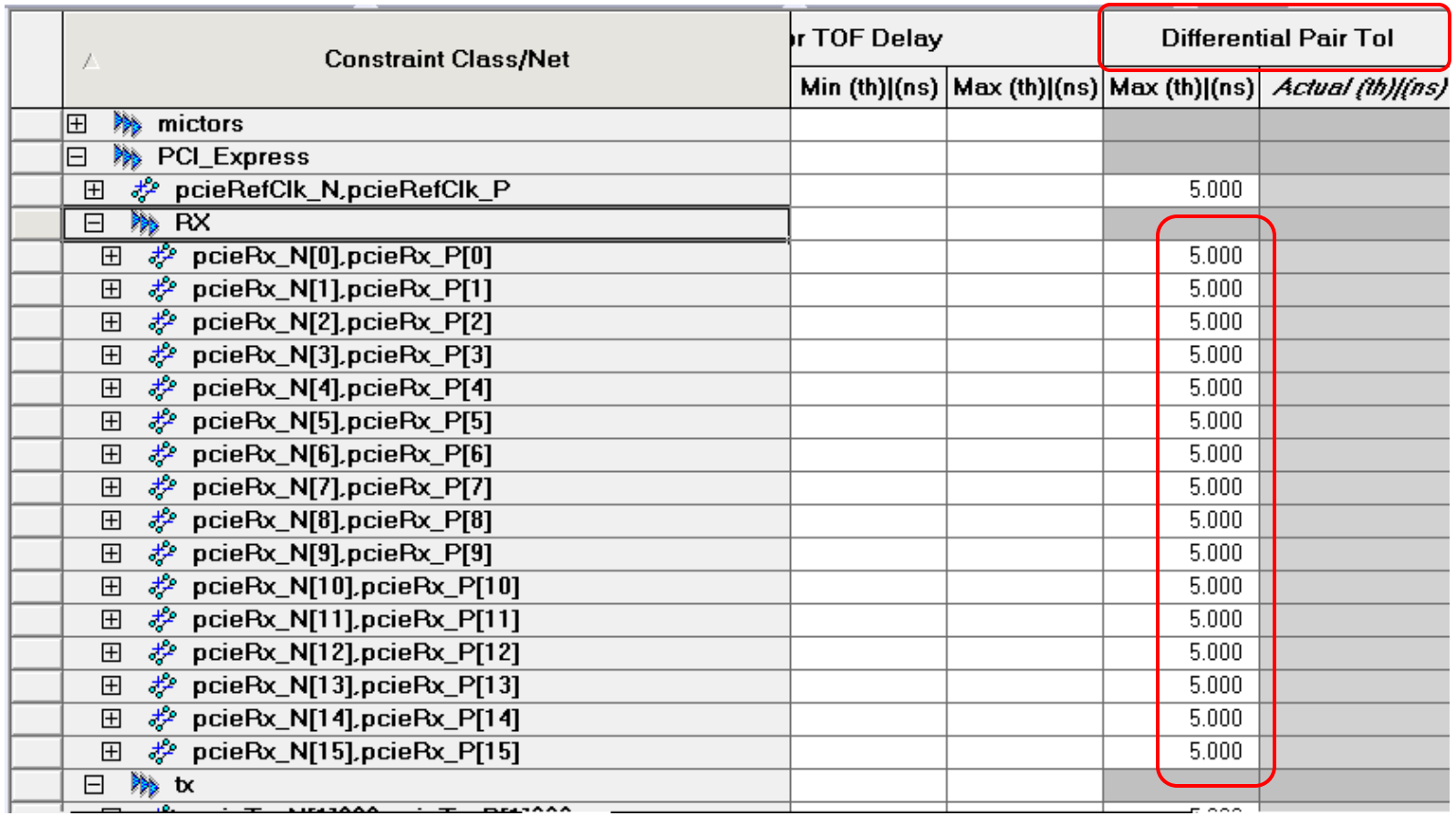


Constraint Manager Tips and Tricks

Differential Pairs

Diff Pair Tolerance

- Match the lengths of P and N signals of the pair within 5 mils
- Do not use the Match Length Column or Formula Column to match the N and P sides.

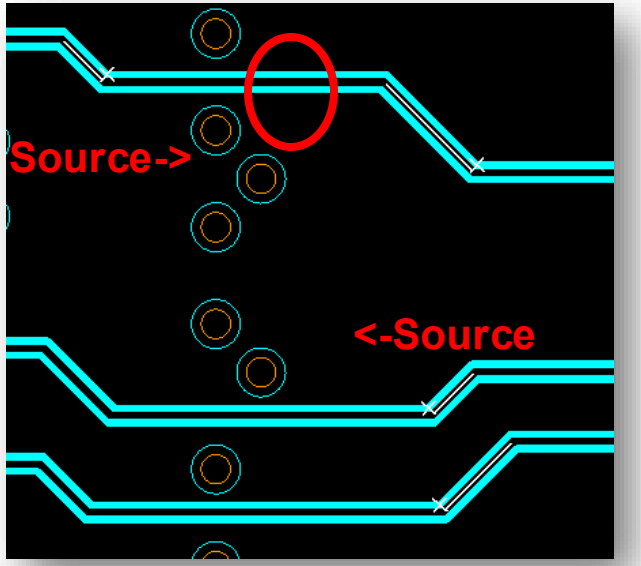


Constraint Class/Net	r TOF Delay		Differential Pair Tol	
	Min (th)|(ns)	Max (th)|(ns)	Max (th)|(ns)	*Actual (th)|(ns)*
⊞ mictors				
⊟ PCI_Express				
⊞ pcieRefClk_N,pcieRefClk_P			5.000	
⊟ RX				
⊞ pcieRx_N[0],pcieRx_P[0]			5.000	
⊞ pcieRx_N[1],pcieRx_P[1]			5.000	
⊞ pcieRx_N[2],pcieRx_P[2]			5.000	
⊞ pcieRx_N[3],pcieRx_P[3]			5.000	
⊞ pcieRx_N[4],pcieRx_P[4]			5.000	
⊞ pcieRx_N[5],pcieRx_P[5]			5.000	
⊞ pcieRx_N[6],pcieRx_P[6]			5.000	
⊞ pcieRx_N[7],pcieRx_P[7]			5.000	
⊞ pcieRx_N[8],pcieRx_P[8]			5.000	
⊞ pcieRx_N[9],pcieRx_P[9]			5.000	
⊞ pcieRx_N[10],pcieRx_P[10]			5.000	
⊞ pcieRx_N[11],pcieRx_P[11]			5.000	
⊞ pcieRx_N[12],pcieRx_P[12]			5.000	
⊞ pcieRx_N[13],pcieRx_P[13]			5.000	
⊞ pcieRx_N[14],pcieRx_P[14]			5.000	
⊞ pcieRx_N[15],pcieRx_P[15]			5.000	
⊟ tx				

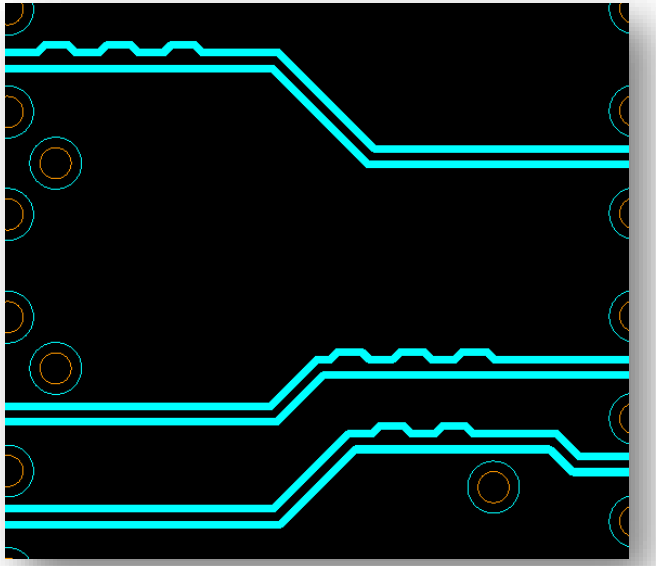
Diff Pair Phase Tolerance

- Max - how far out of phase the signals of the differential pair are allowed to get.
- Distance Max - how much further the two signals can continue running out of phase after exceeding the Differential Pair Phase Tol Max constraint.
- X icon indicates the source side

	Differential Pair Phase Tol		
	Max (th)	Distance Max (th)	*Actual*
	50.000	100.000	
	50.000	100.000	*No Violation*



As the signals go around the bend
they get out of phase

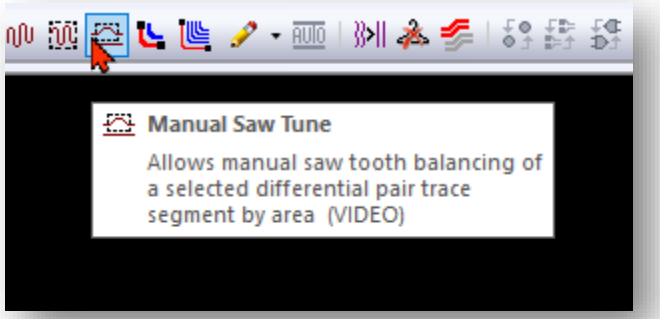


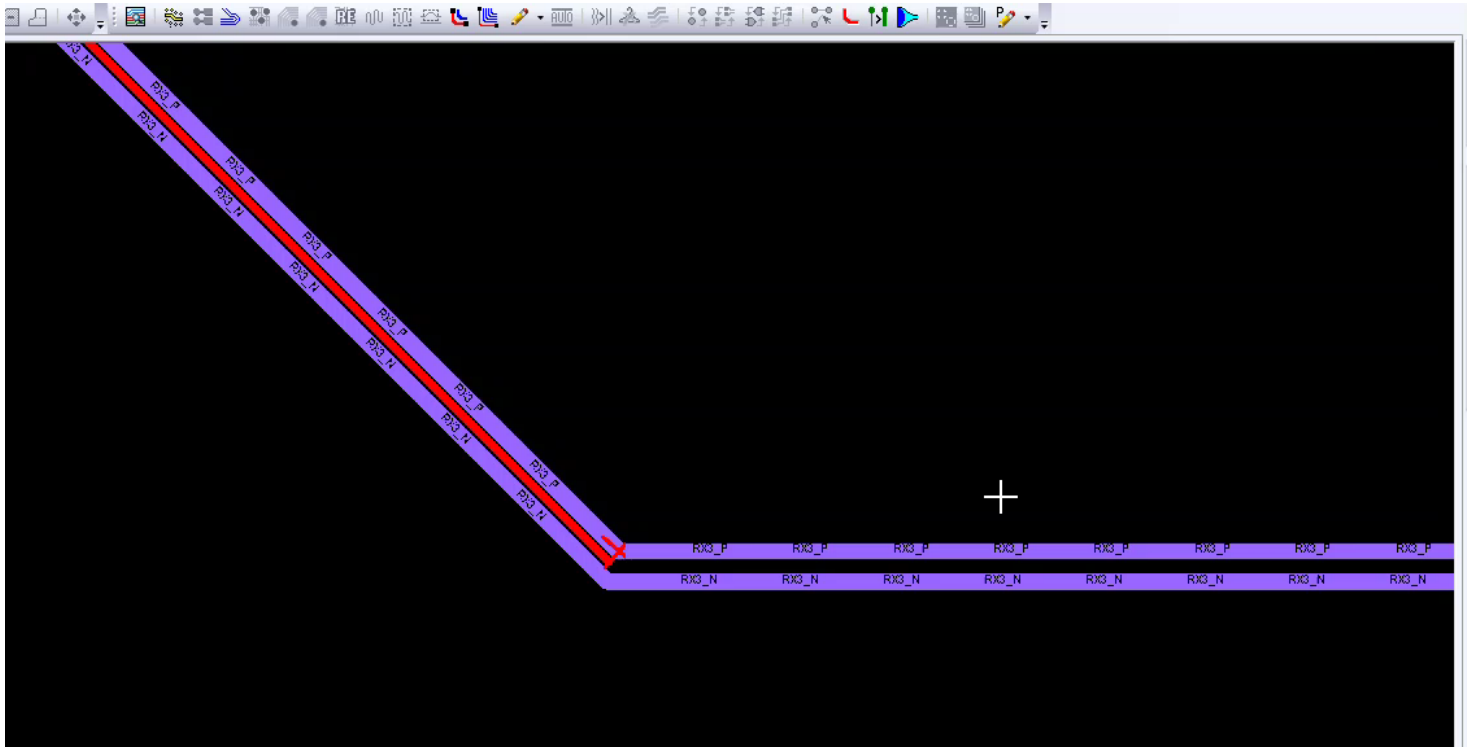
Saw Tune used to get signals in phase

Phase Tolerance Example

Differential Pair Phase Tol	
Max (th)	Distance Max (th)
5	100
5	100
5	100
5	100

If Traces go out of phase by 5 mils AND they stay out of phase for 100 mils (or more) – flag a violation





Manual Saw Tune on the LOAD side.

TEŞEKKÜRLER

CDT TECH DAY