CDT TECH DAY

MAY 28th

CDT techday'e hoş geldiniz

Questa One

Transforming Verification from Complexity To Clarity

Faïçal Chtourou
Filed Application Engineer

SIEMENS

Agenda

Why, What **Questa One**

Questa One in a nutshell

- **Questa One** Sim
- **Questa One** SFV
- **Questa One** VIQ
- **Questa One** Avery VIP

Deep Dive **Questa One** Sim

Why, What
Questa One

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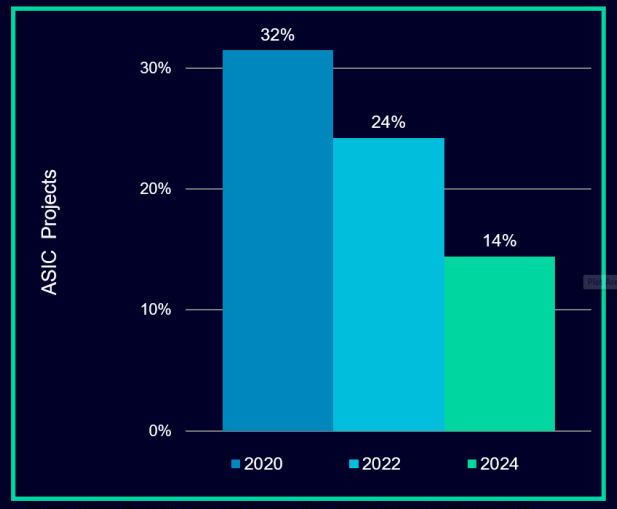
Why Does It Matter?

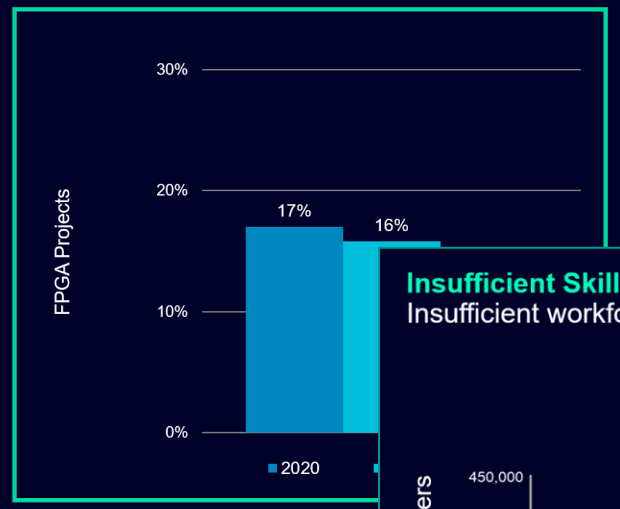
First Silicon Success Declining

Decline in ASIC first silicon success and increase in FPGA no non-trivial bug escapes

ASIC First Silicon Success



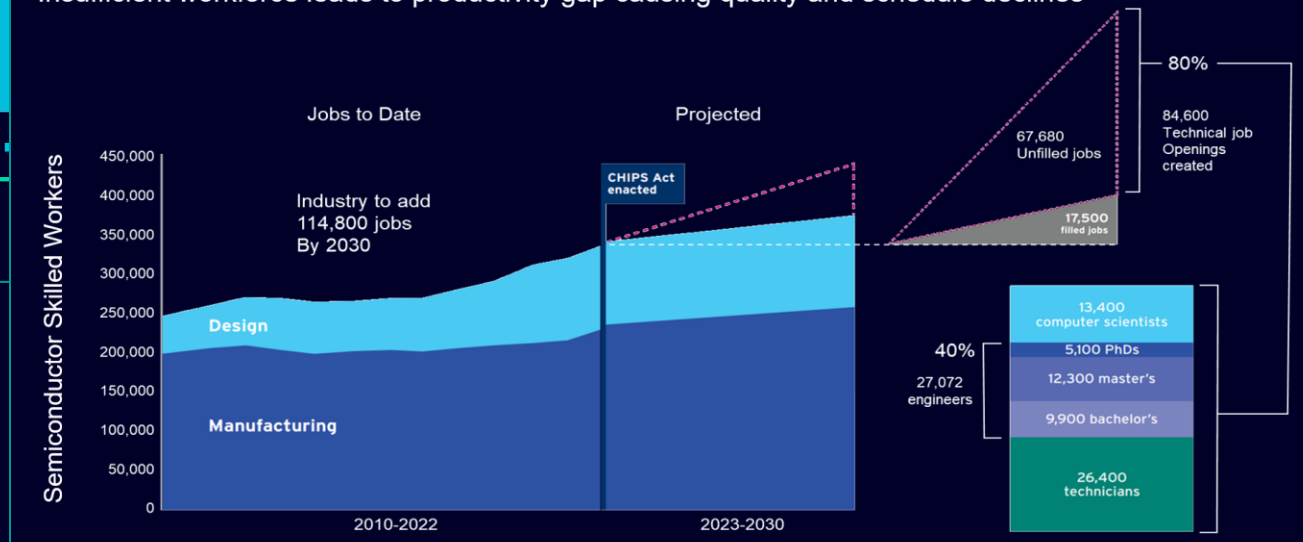
FPGA No Bug Escapes



Source: Siemens EDA and Wilson Research Group, 2024 Functional Verification Study

Insufficient Skilled Workforce

Insufficient workforce leads to productivity gap causing quality and schedule declines



Source: Semiconductor Industry Association (SIA), in partnership with Oxford Economics Study, July 2023

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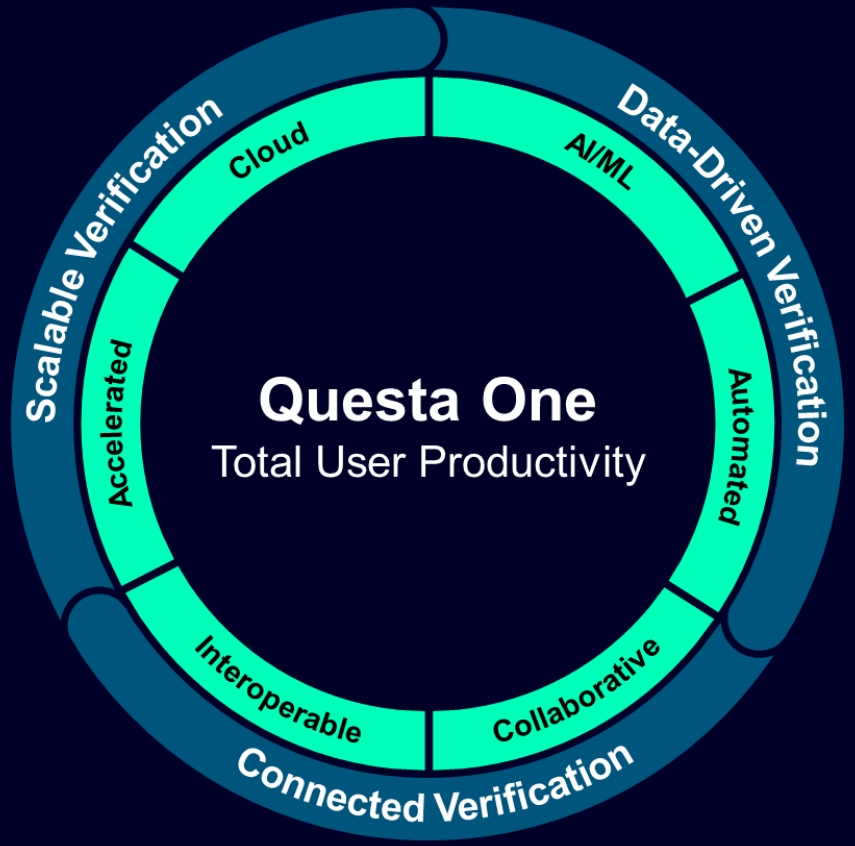
Questa One – Next Generation of Smart Verification Solution enabled by AI
Improving user productivity through the collective power of technology



Faster Engines ▲

Faster Engineers ▲

Fewer Workloads ▲

Delivering up to **5x** improved
Total User Productivity

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Questa One Smart Verification Solution enabled by AI

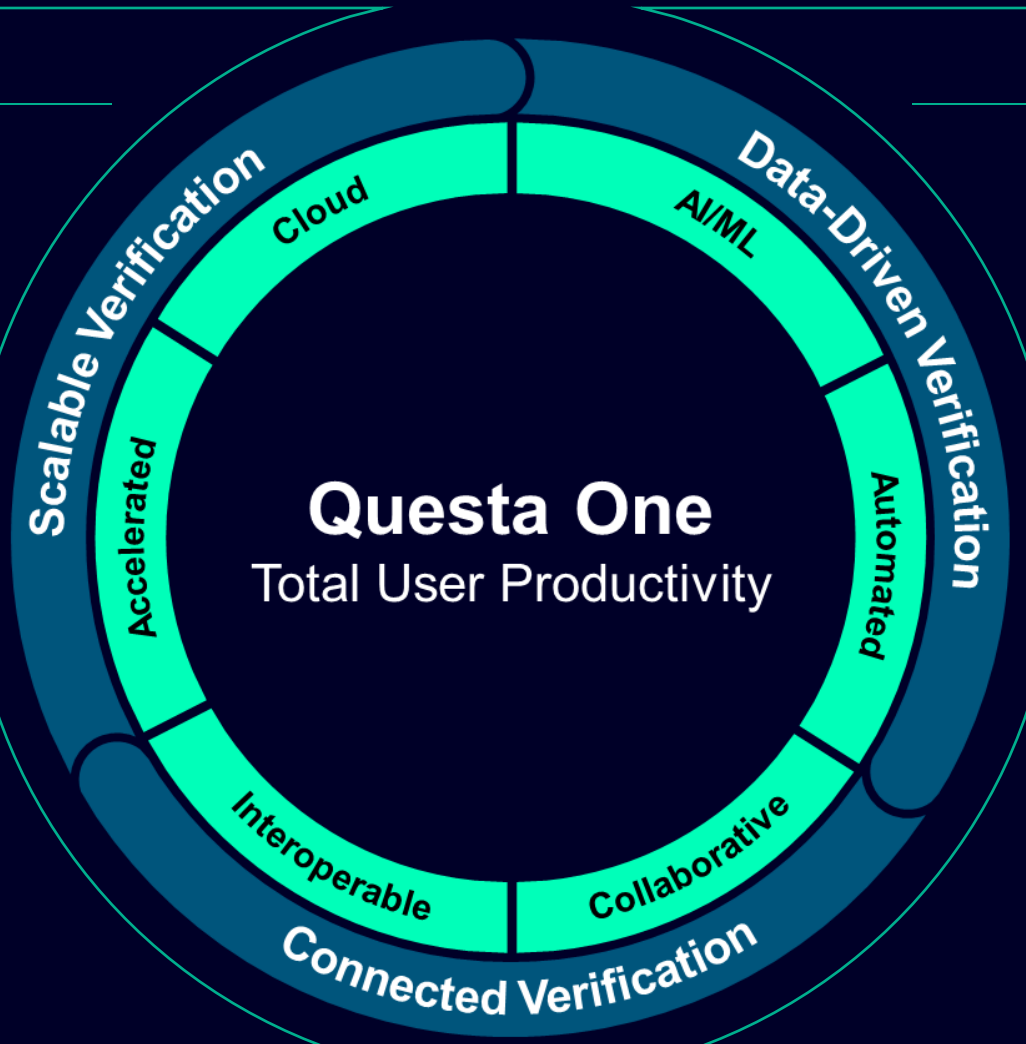
Faster engines, faster engineers, fewer workloads

Questa One Sim

One engine with breakthrough performance for functional & fault sim for RTL, GLS, & DFT applications with parallel processing & profiling

Questa One Verification IQ

One smart common coverage solution that utilizes generative, analytic, & predictive AI to drive to verification closure faster, with fewer workloads



Questa One SFV

One stimulus free verification solution delivers total user productivity by combining static & formal analyses through AI, automation, & parallelization

Questa One Avery VIP

One industry-leading VIP solution that supports 3DIC & chiplet verification from IP to SoC, seamlessly integrating simulation & emulation

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Questa One
Verification IQ

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Analytical AI | Predictive AI | Generative AI

QuestaTM One Smart Verification

Faster engines, faster engineers and fewer workloads

Smart Creation

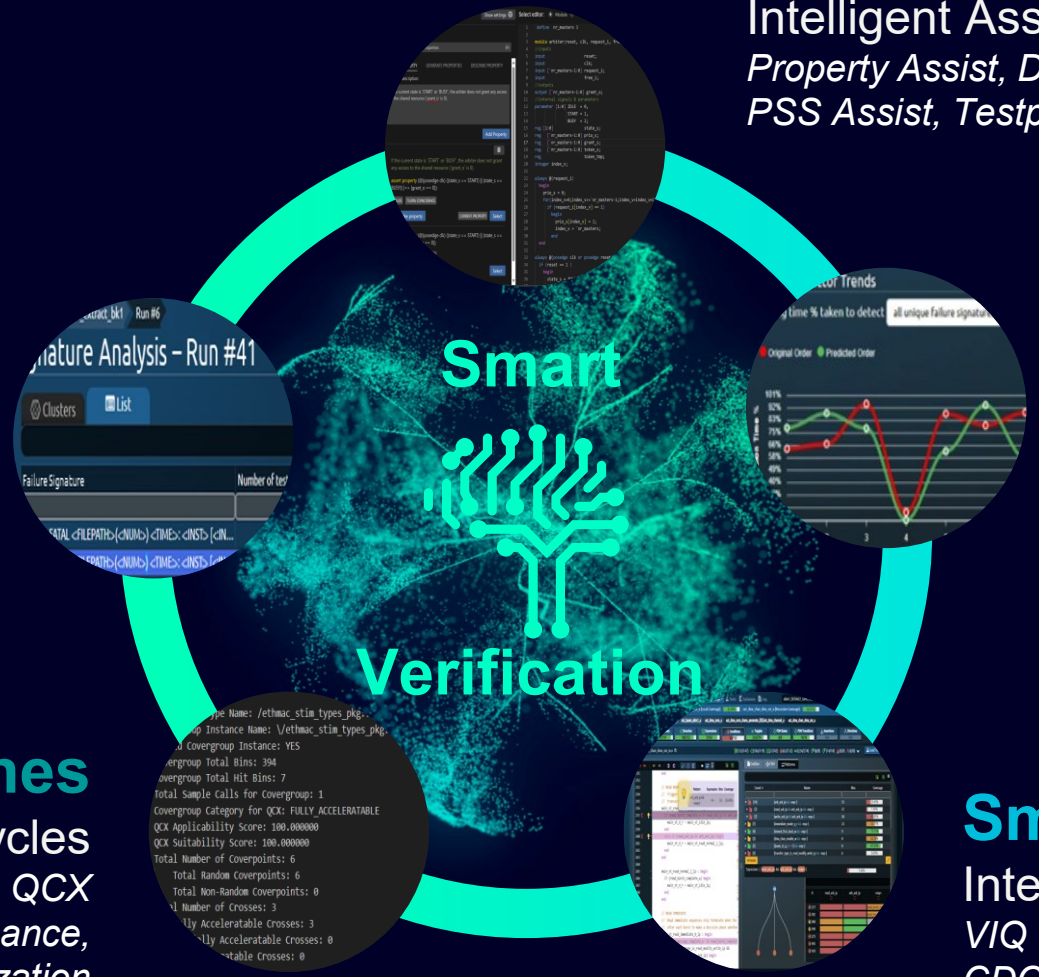
Intelligent Assistance

Property Assist, Docs Assist, PSS Assist, Testplan Assist, Code Assist

Smart Debug

Intelligent Root-cause

VIQ Regression Navigator – Signature, Bad-commit & Root-cause Prediction, *Protocol Assist*



Smart Regression

Optimized Regression Cycles

VIQ Regression Navigator - Failure, Smoke-test & Schedule Prediction

LOAD

Smart Engines

Intelligent Verification Cycles

QCX

Questasim Performance, Coverage Optimization

Smart Analysis

Intelligent Insights

VIQ Coverage Analyzer, CDC Assist & RDC Assist

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Questa One SFV

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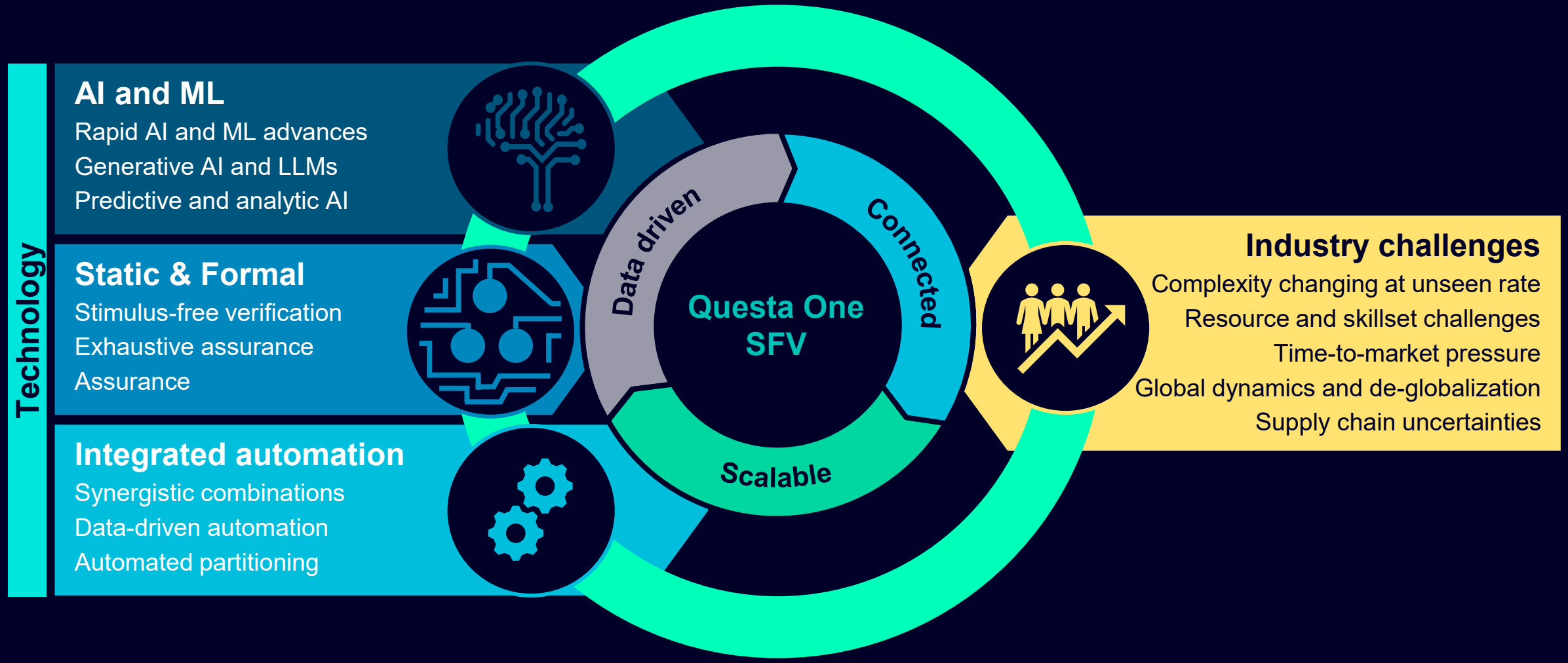
Introducing Questa One SFV: Purpose-built stimulus-free verification

AI/ML, automation and integration enable new high-productivity flows and solutions



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Questa One Avery VIP

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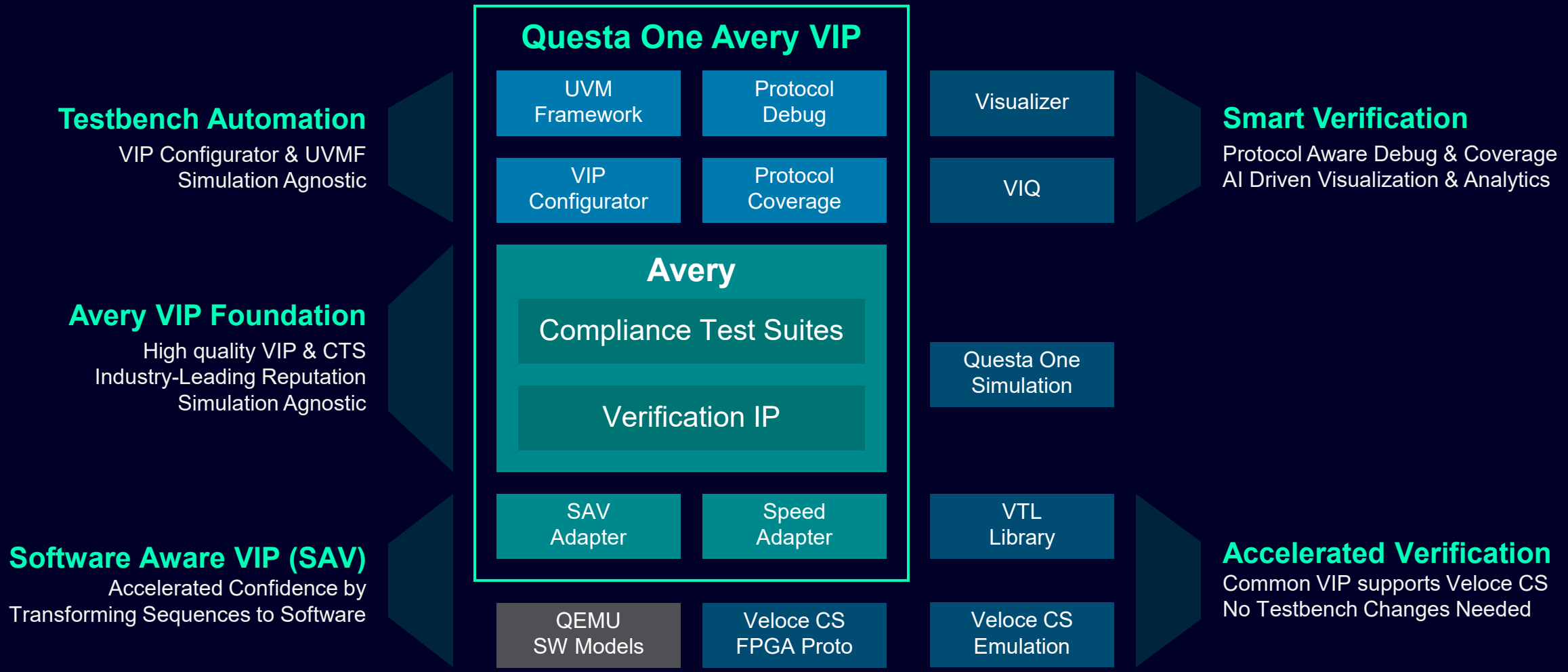
Questa One Avery VIP
Expanding the power of Avery through solution ecosystem



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Questa One Simulator

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Questa One Simulator

Purpose built to meet the productivity demands of the industry

IEEE
UVM
UPF UNIFIED POWER FORMAT
SystemVerilog
SYSTEMC
PORTABLE STIMULUS
VHDL-2019
MathWorks
ocotb
UVVM
OSVVM

Siemens Questa One Simulator

Faster Engines

- New Engine
- ParallelSim with Auto-partition
- New Coverage Engine
- FuSa

Faster Engineers

- NextGen Profiler
- Intelligent Debug
- Metastability analysis
- Static & Dynamic Power Analysis

Fewer Workloads

- Coverage Acceleration
- DFT Acceleration
- SmartCompile
- Unreachability Analysis

Scalable Verification

Data Driven Verification

Connected Verification

AARCH 64
x86
aws

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Deep Dive into
Questa One Sim

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Questa One Simulator

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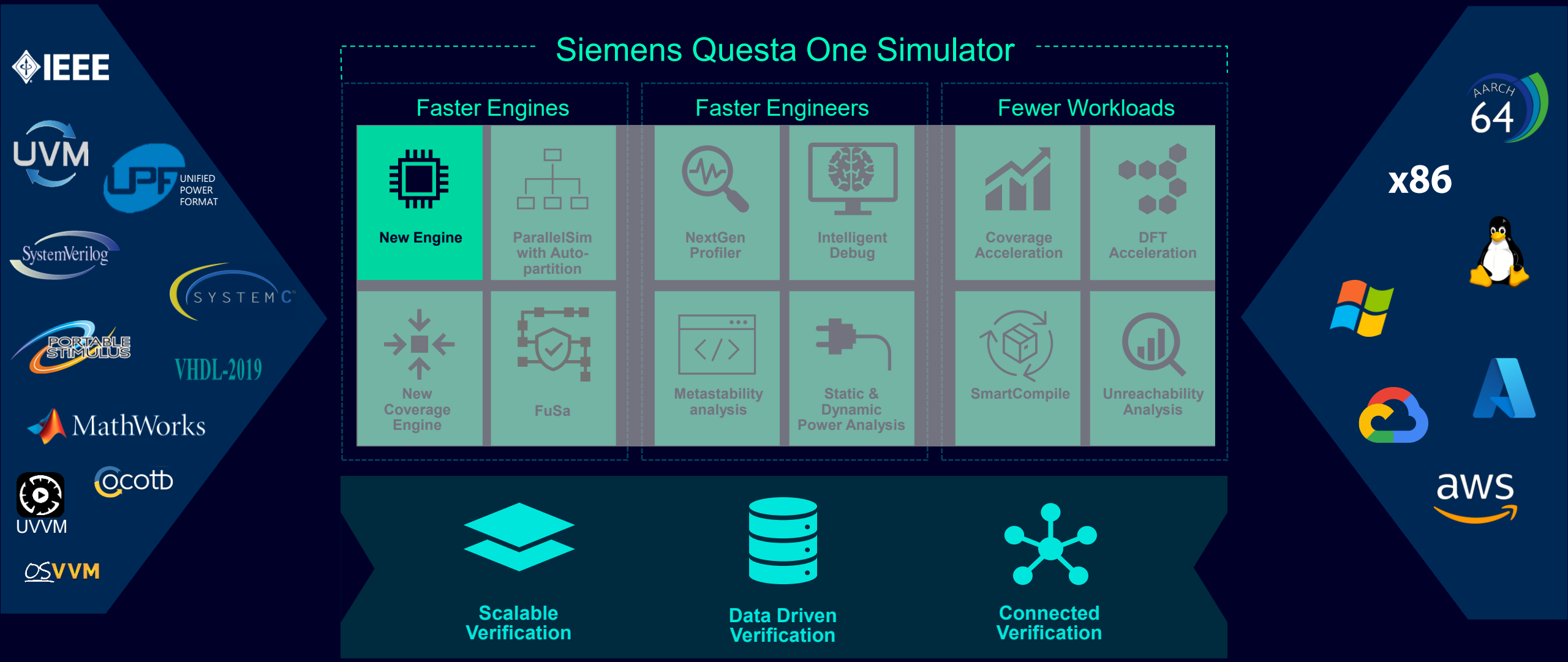

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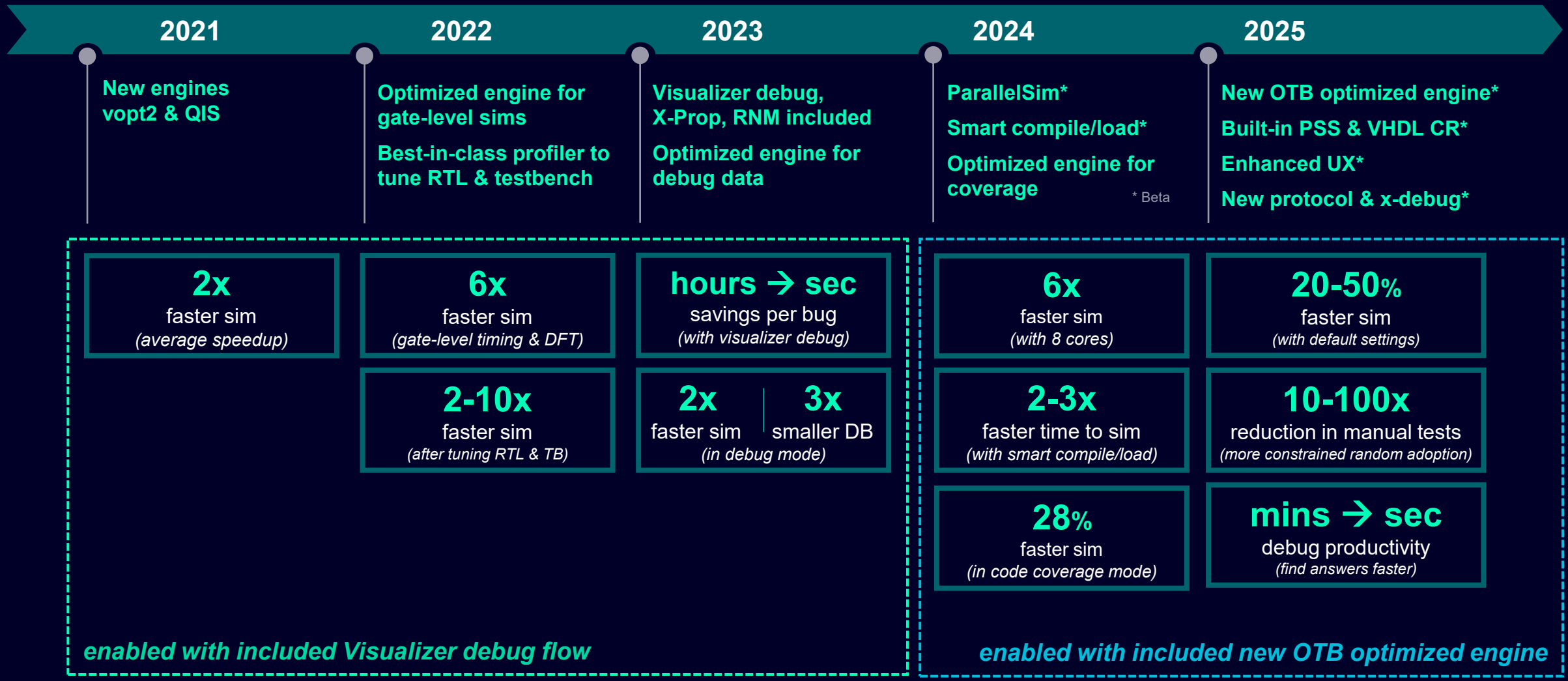
Questa One Sim
Investments that brought us here



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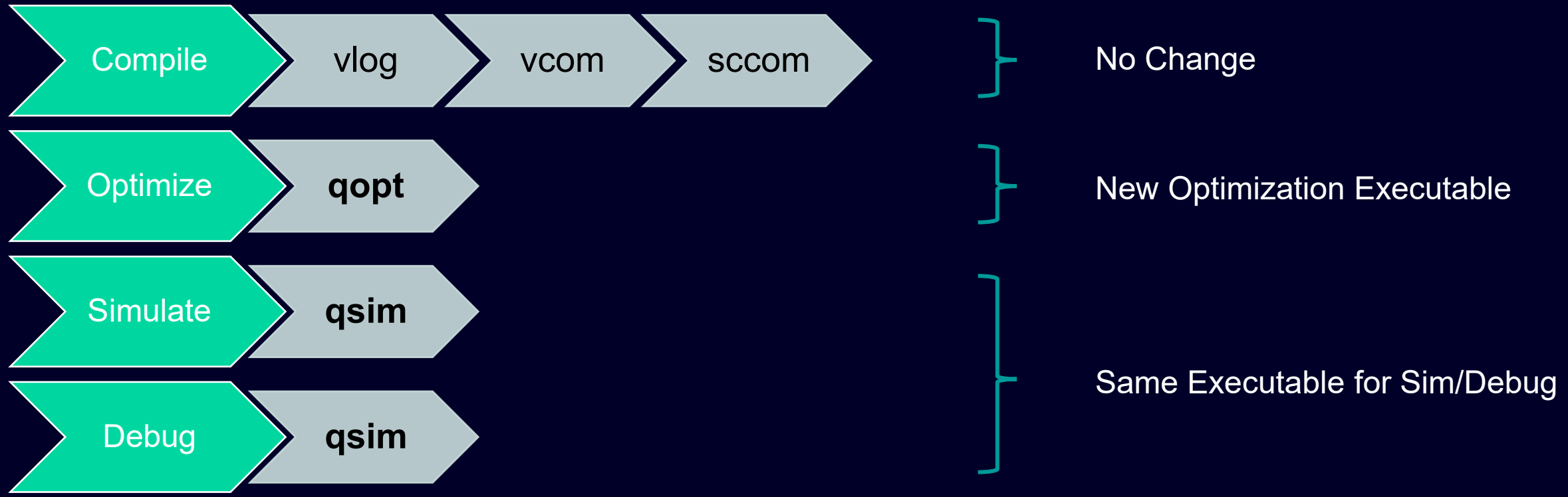
Definition
New Executables for Questa One Sim



Same package as Questa Sim Prime

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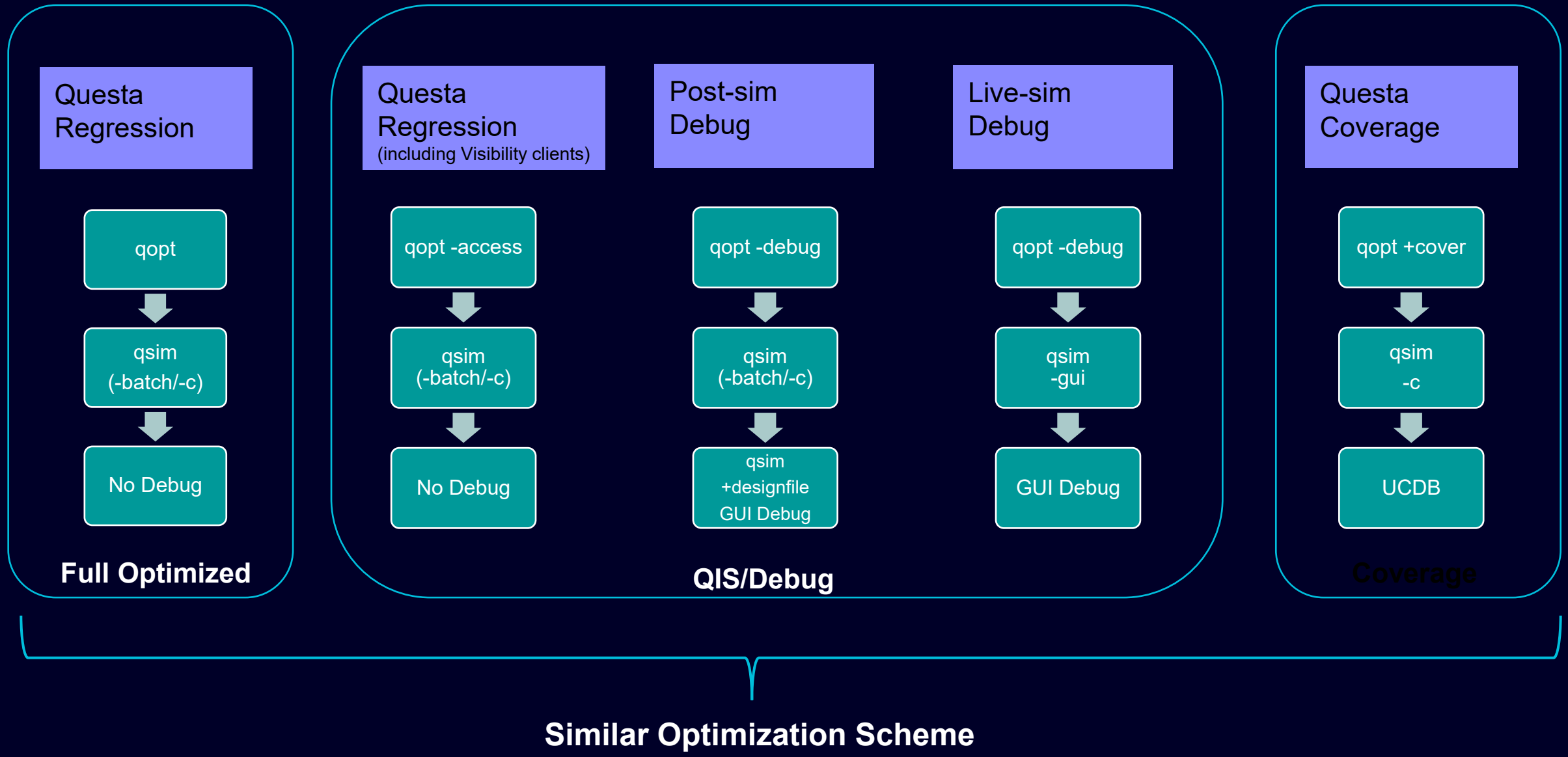
Why? Simulation Behavior Consistency



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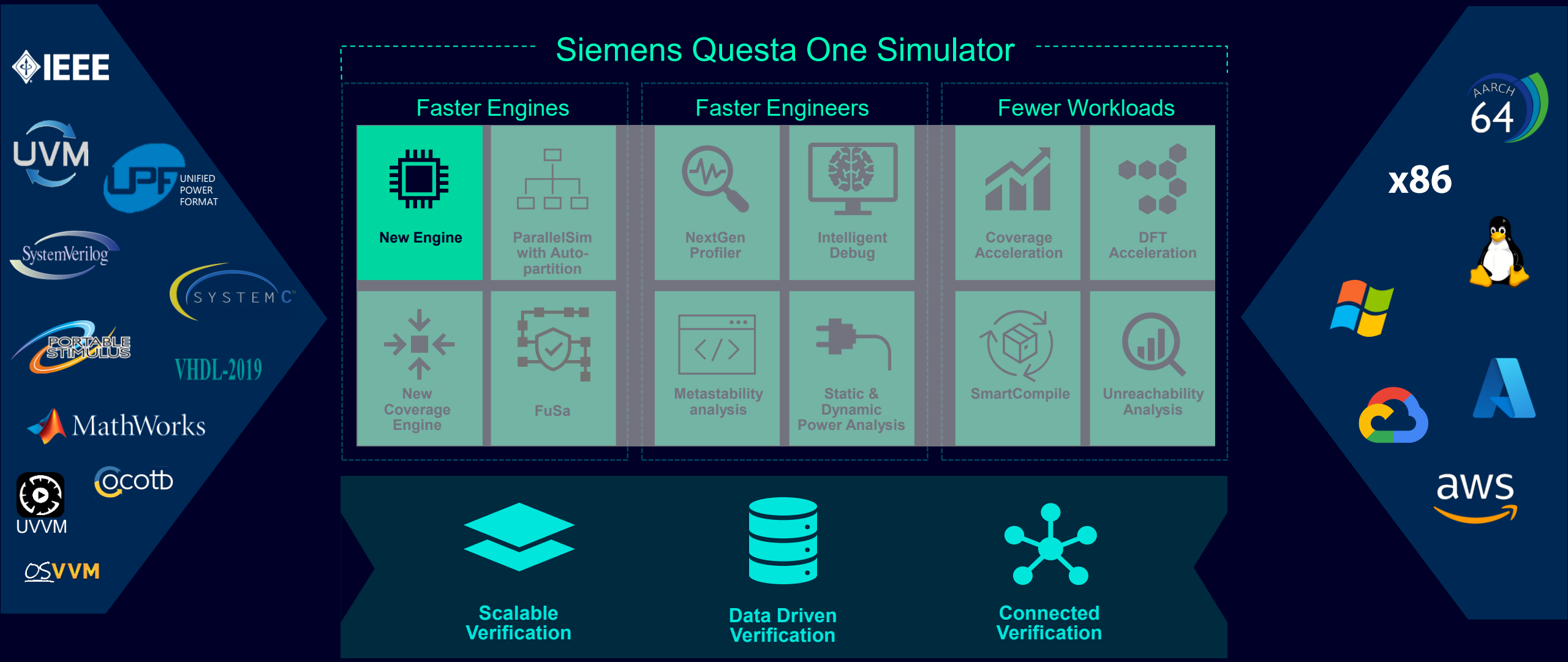
General Use Model Examples

Use Model	Legacy Executables	New Executables	Details
General Purpose run	vlog/vcom/sccom vopt vsim	vlog/vcom/sccom **qopt** **qsim**	• User should change to qopt/qsim to open Questa One Sim features
How to open GUI "Live-sim mode"	vlog vopt +acc vsim -gui -do "add log…"	vlog qopt **-debug -designfile…** qsim -gui -do "add log …"	• +acc is hard error • User should add -debug, -designfile • -gui will invoke Questa One Sim GUI (Live-sim mode) • design.bin file will be located and loaded • Qwave dumping is enabled upon "add log" or through -qwavedb
How to open GUI "Post-sim mode"	vsim -view vsim.wlf visualizer -wavefile -designfile	qsim –wavefile -designfile	• -view is not supported • qsim follows Visualizer operation for backward compatibility
qsim Default Mode "without top"	vsim -do "…"	qsim -do "…"	• Invokes Questa One Sim GUI in (Frame-work (IDE) mode)
qsim Default Mode "with top"	vsim top_opt	qsim top_opt	• Open Questa One Sim GUI (Live-sim mode)
Visibility Clients	vopt +acc	qopt **-access=…**	• Same use-model as QIS
Regressions Mode	vsim -c	qsim -c	• New -console technology is loaded automatically

Questa One Simulator

Purpose built to meet the productivity demands of the industry



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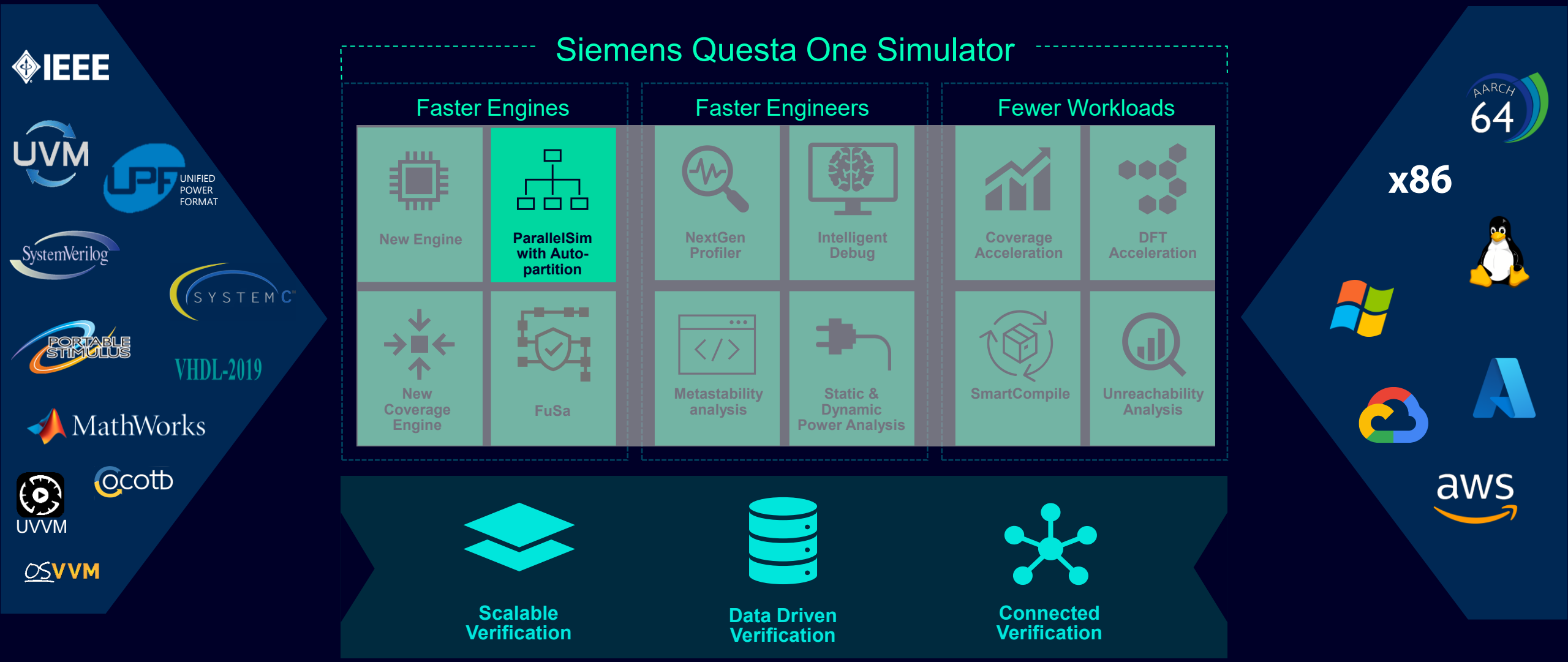
Questa One Simulator

Purpose built to meet the productivity demands of the industry



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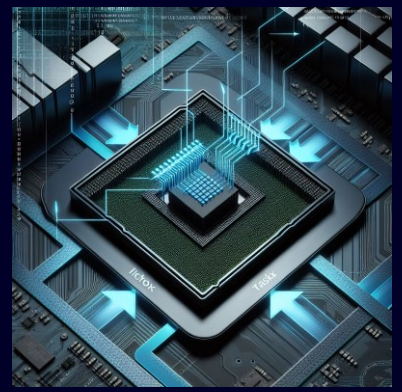
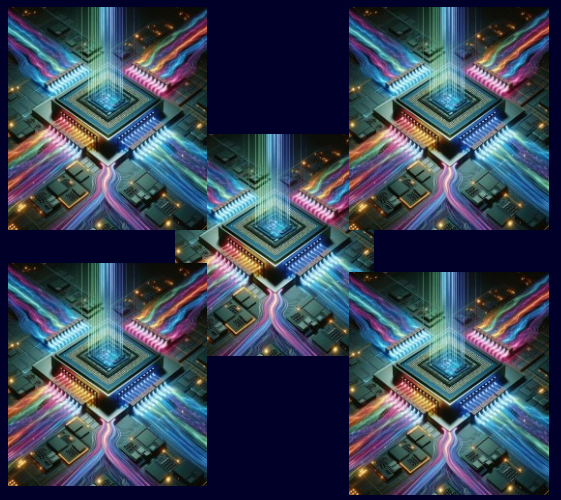
ParallelSim
What is ParallelSim?

- ParallelSim is a multi-core simulation to achieve performance acceleration
- ParallelSim automatically partitions the design at fine-grained level
- Runs each partition in parallel to achieve better performance
- Leverage existing Questa licenses to run on multiple cores
- Preview design fit with Questa Profiler



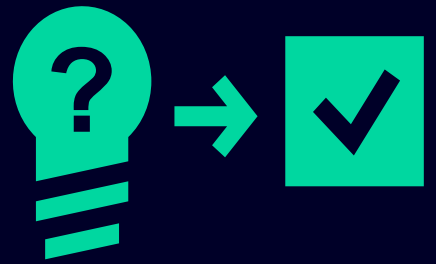
Questa Single-core simulator



Questa ParallelSim using multiple cores

ParallelSim
How does the user know?

- That the design is suitable for ParallelSim and can achieve dramatic performance results?
- What is the number of cores that will get the best performance results?



So, it is important to qualify the design first and decide if it fits well with ParallelSim or not.

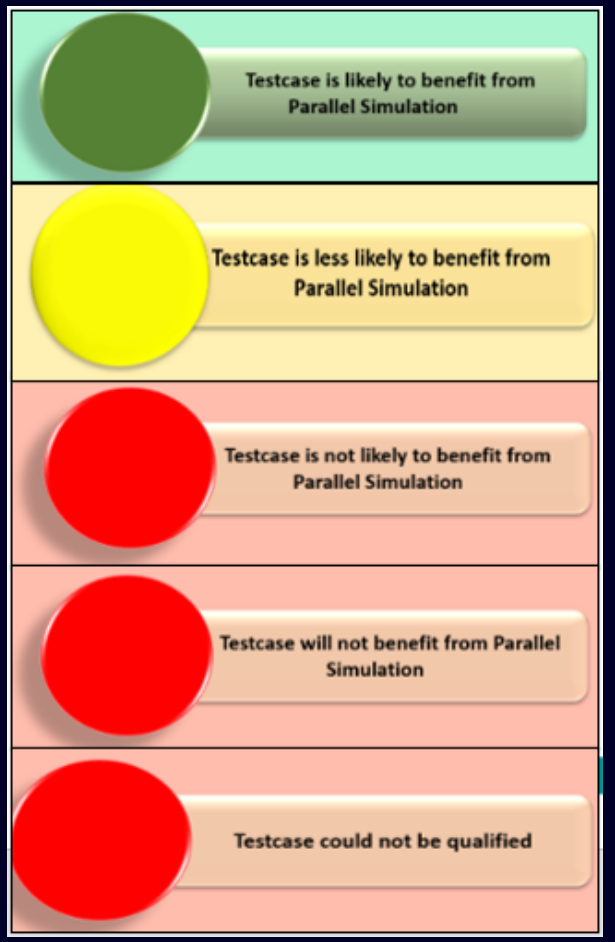
Use ParallelSim Qualifier

ParallelSim Qualifier
What is it?

- ParallelSim Qualifier is a profiler utility that helps with the following :

1. Determines if a given design will be applicable for parallelism or not.
2. Recommends the best number of partitions to run on our design.
   → –flps=<the number of partitions> <qualifier recommended options>

Qualifying the design



ParallelSim Qualifier conclusions

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ParallelSim Qualifier
How to Run?

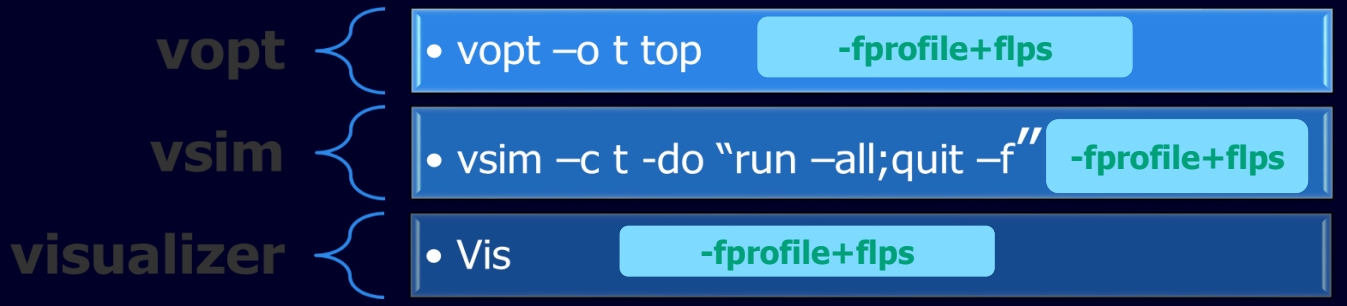
- Add –fprofile+flps option to qopt & qsim command line
- Use –fprofile+flps with visualizer to invoke qualifier analysis client

- Same options with all the flows :

Flows

- **Qrun flow**
  qrun -fprofile+flps
- **3-step Flow**
  qopt top -o opt -fprofile+flps
  qsim -c opt -do "run -all; quit -f" -fprofile+flps
- **2-step flow**
  qsim -c top -do "run -all; quit -f" -fprofile+flps
- **ELAB flow**
  qopt top -o opt -fprofile+flps
  qsim -c opt - -fprofile+flps -elab ....
  qsim -c opt -fprofile+flps -load_elab ...

Qualifier also works with vopt/vsim



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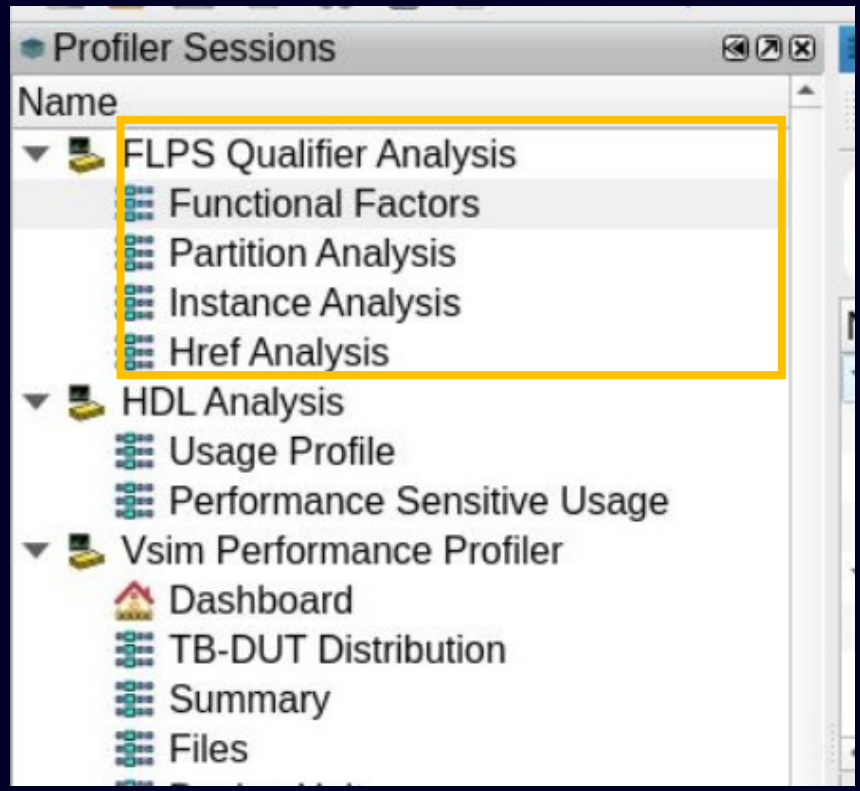
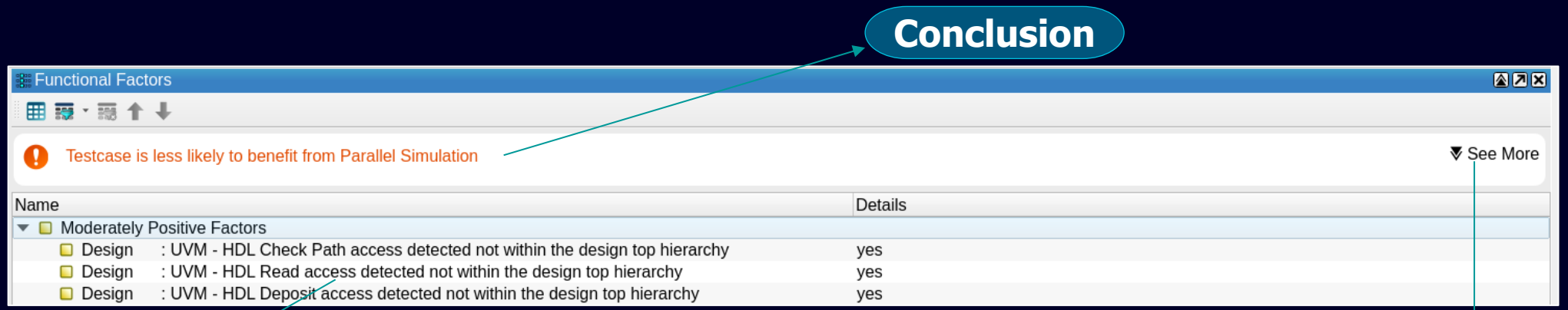
ParallelSim Qualifier
What data does it show?

- **Main QUALIFEIR ANALYSIS Windows:**
  - Functional Factor window
  - Partition analysis window
  - Instance analysis window
  - Href Analysis Window



Functional Factors Window

- The Functional Factors window lists the factors that contributed to the Negative or Moderately positive/negative conclusion. This is also main window to review Qualifier conclusion details.



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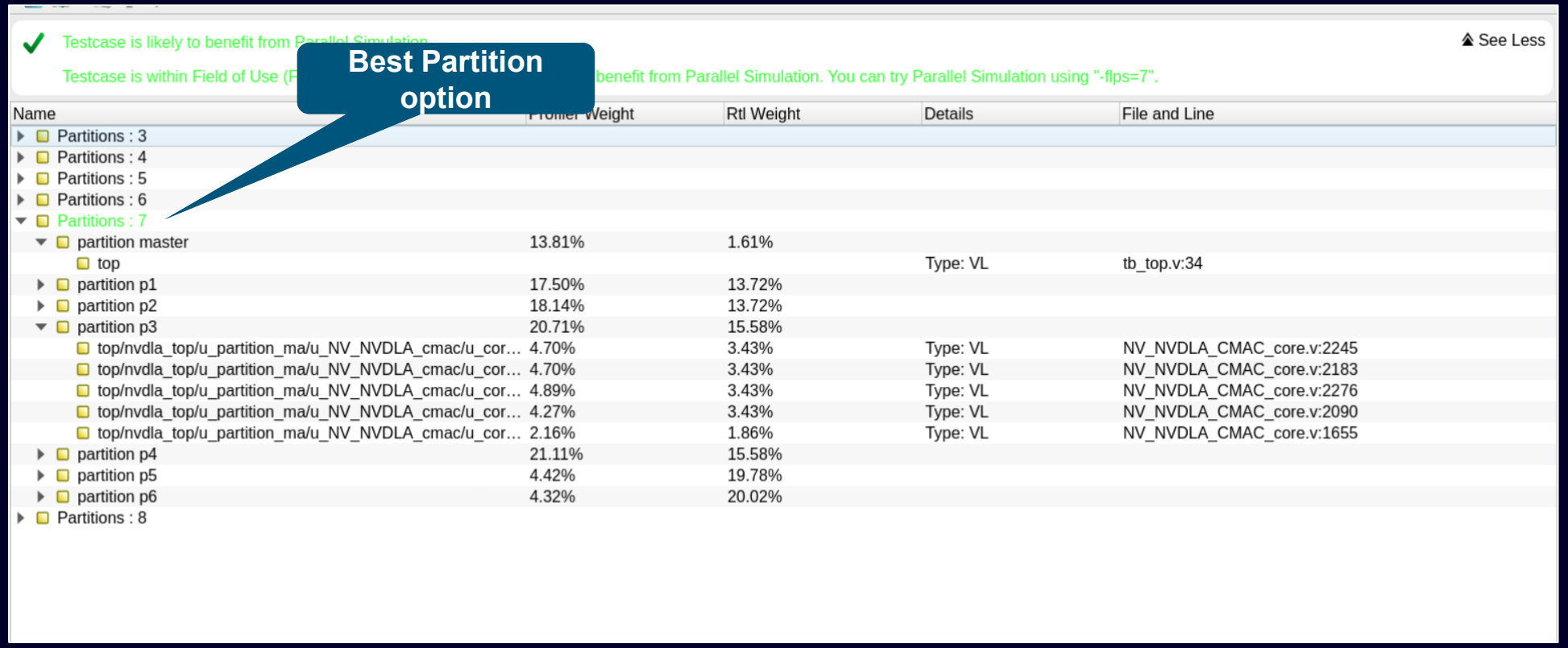
Partition Analysis Window

- It gives an insight on the trials that the qualifier did on partitioning the design.
- The best number of partitions (if it exists) appears in green.
- The following information is provided for every partition:
  - Profiler Weight
  - RTL Weight



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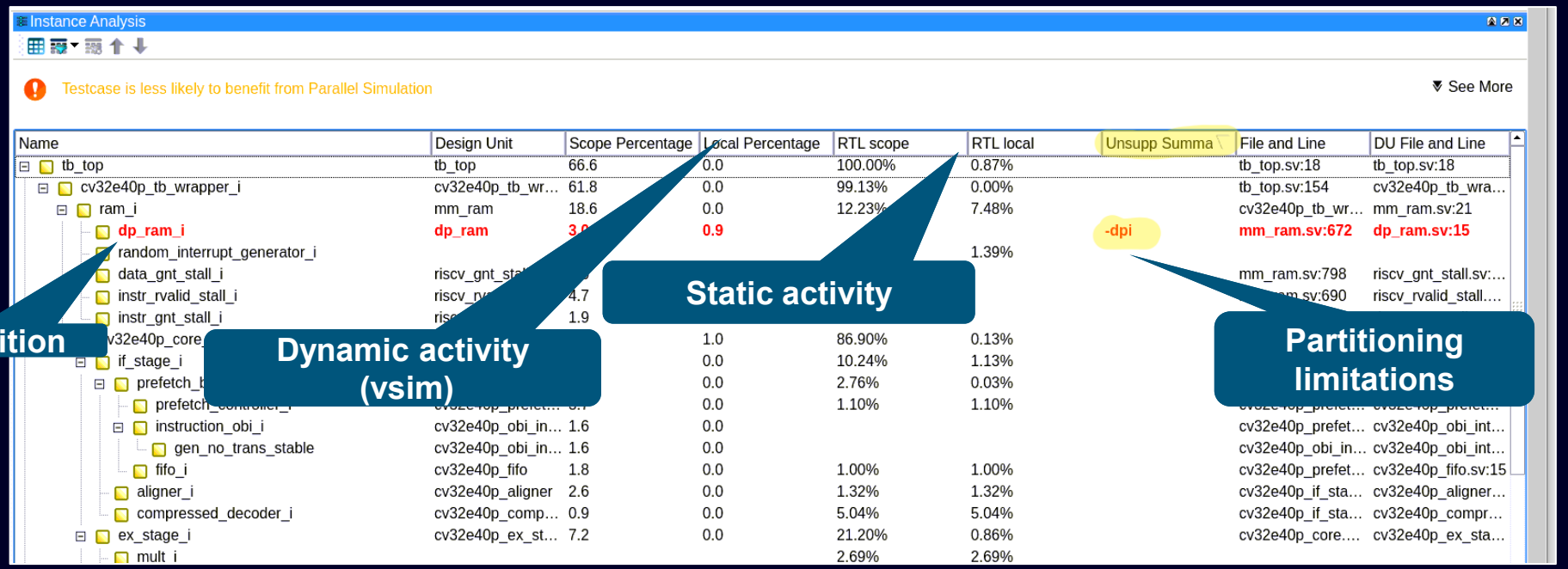
Instance Analysis Window

- The Instance Analysis window provides a tree view of the design structure.
- The following information is provided for every instance in the design tree:
  - Design Unit
  - Scope/Local percentage
  - RTL scope/local percentage
  - File and line of instantiation
  - DU File and line
  - Unsupp Summary



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ParallelSim
How to Run?

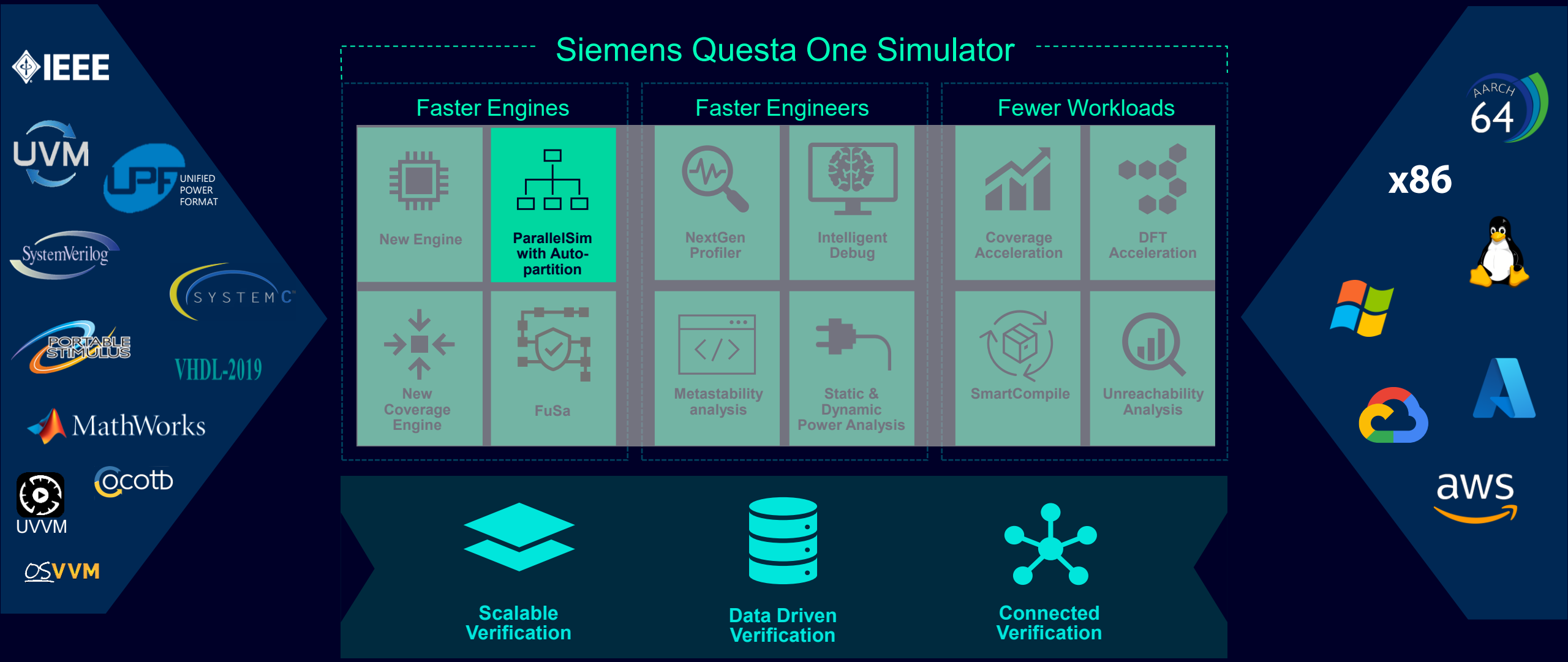
- Add –flps=<n> option to qvopt & the other qualifier recommended options.
- Add –flps option to qsim.
- For debugging, visualizer can be opened as usual.

qopt
- qopt –o t top **-flps = <n> <recommended options>**

qsim
- qsim –c t –do **-flps** “run –all”;quit –f”

Questa One Simulator

Purpose built to meet the productivity demands of the industry



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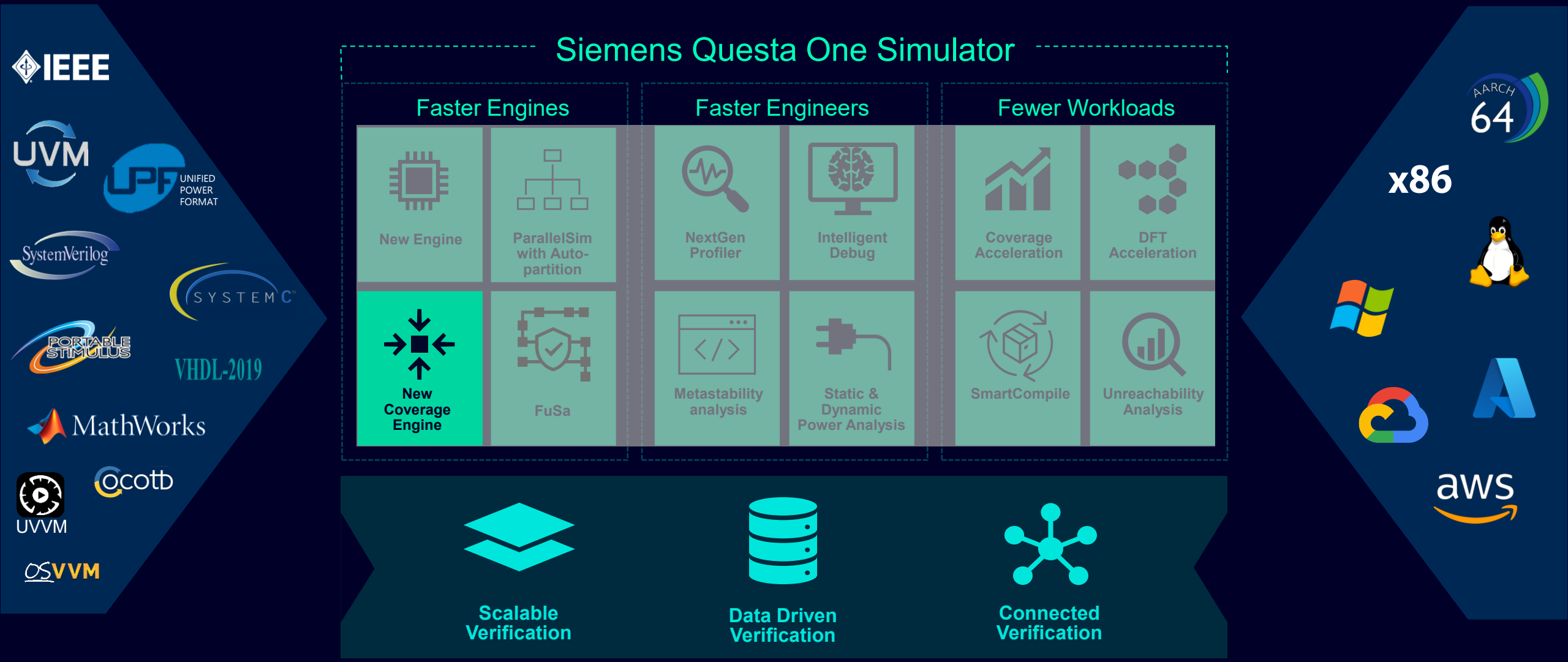

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What is Ngcoverage

Next Generation Code Coverage Engine

- **Faster Performance**
  - More optimizations
  - Performance oriented defaults
    - Turn on the extra coverage you need
- **Consistency**
  - Always create bins based on user code, not optimizations
  - Better Match fully optimized behavior
    - Less race condition differences
- **Smarter Architecture**
  - Enable new enhancements and tools

28%

faster sim

(in code coverage mode)

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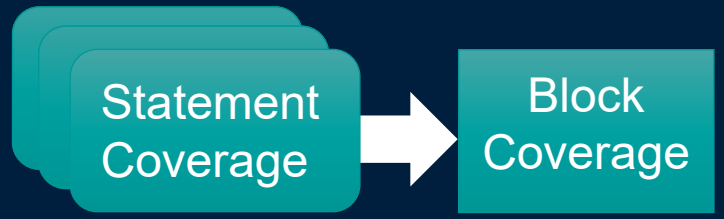
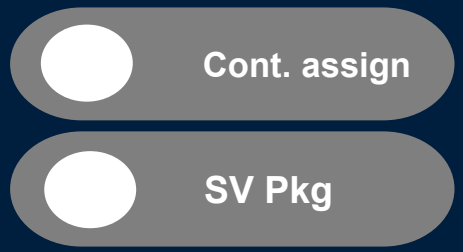
Next Generation Coverage
-ngcoverage efficiency & consistency

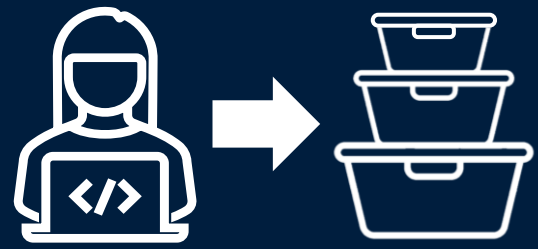
Reduced Data Size
Less storage space.
Faster merge and analysis

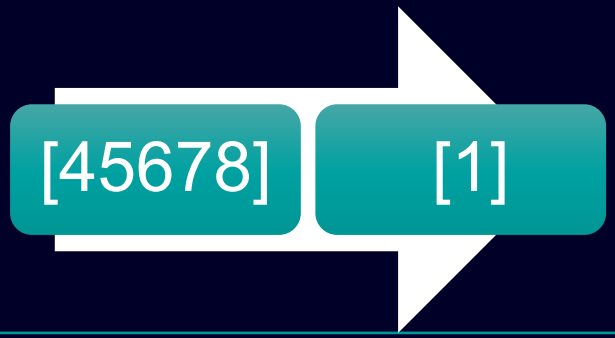
Better Defaults
Many coverage constructs are now off by default

Consistent Bins
Always create bins based on user code, not optimizations









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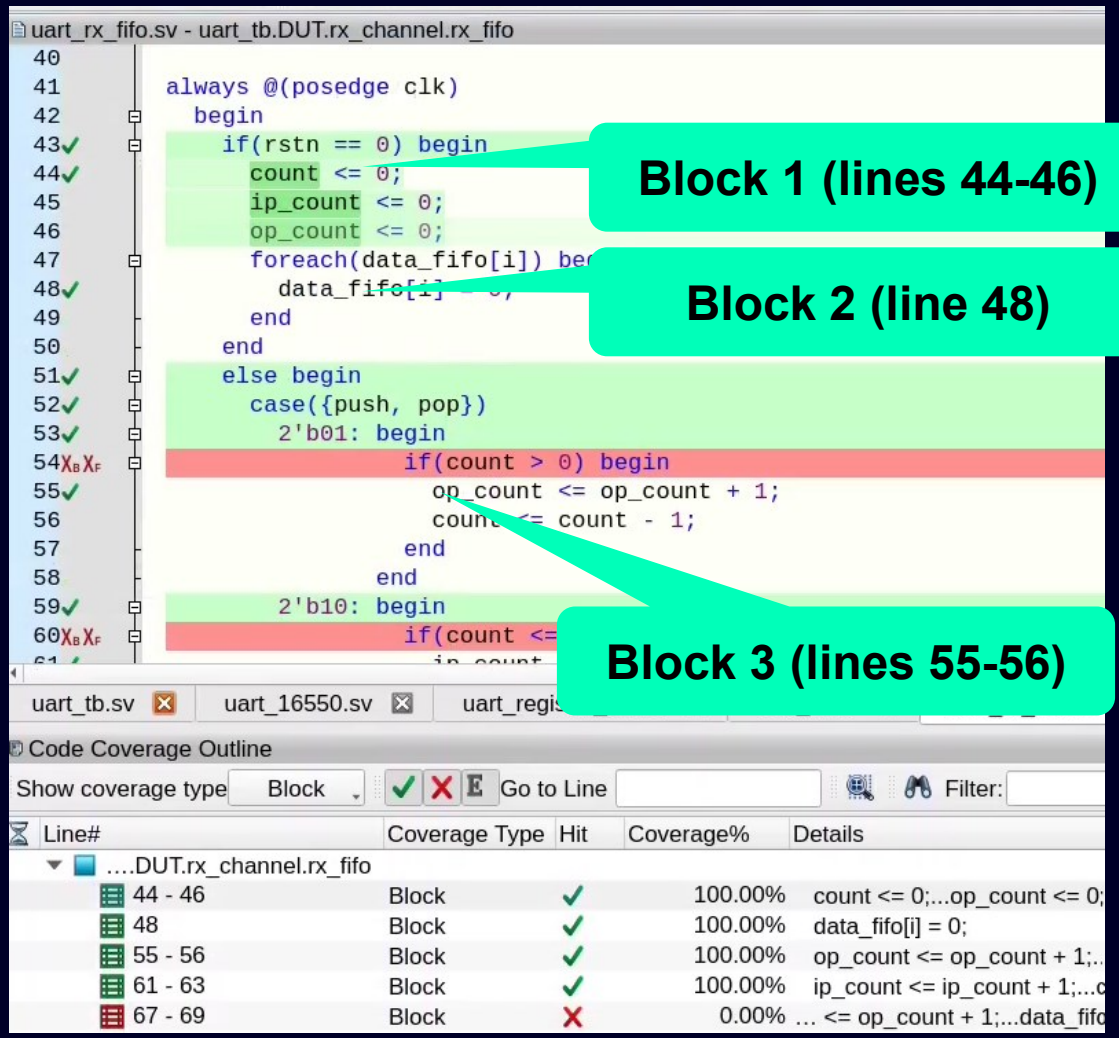
Block Coverage

Block Coverage

- Block coverage replaces statement coverage
- A block is a group of statements with a single entry and exit point such as:
  - begin-end, if-else, case, wait, while loop, for loop etc.
- Block coverage measures each group of statements executed
- Same exclusion syntax. Exclude any line in the block, exclude the whole block.



Questa One Sim - New Code Coverage Defaults

- Questa One Sim
  - Code Coverage engine is ngcoverage

  - qopt +cover
  - qsim -coverage -do “coverage save onexit name.ucdb

  - Post-sim Flow changes
    - vsim -c -viewcov -> qsim -c -viewcov
    - vis -viewcov -> qsim -viewcov

- Questa Core/Prime 2025.2
  - No Change to defaults

Questa One Sim (ngcoverage) Coverage Migration Guide

qopt +cover
qsim -coverage -do “coverage save onexit name.ucdb

- Post-sim Flow changes
  - vsim -c -viewcov -> qsim -c -viewcov
  - vis -viewcov -> qsim –viewcov

- UCDB compatibility
  - No format change.
  - Questa One gui/Visualizer/VIQ/"vsim -c" readers all work.
  - TK GUI does NOT support ngcoverage

- Merge – code coverage must match engine
  - “code coverage” from legacy NOT merge compatible with ngcoverage
  - “vopt +cover -ngcoverage” ↔ “qopt +cover” OK

Questa One Sim (ngcoverage) Coverage Migration Guide
optimization for best performance

- Change **vopt** → **qopt**

- Remove +acc switches.
- Remove -coveropt
- **Remove -inlineFactor=0**
- Remove -covermode
- Add -coverconstruct only if you need them

- The best coverage performance is now out of the box

- And just like before: Limit +cover to the hierarchy/coverage types necessary, and -toggleportsonly if you only need toggle ports.

Questa One Sim (ngcoverage) Coverage Migration Guide
Exclusion Commands Migration

Toggle Exclusions

- No change is required to the exclusion commands.
- Note: Toggle nodes may have additional alias nodes

```
coverage exclude -du <du_name> -togglenode <node_name>
```

Block Exclusions

- No change is required to statement exclusion commands
- Note that when applying an exclusion on a line/statement that's a part of a block, the whole block gets excluded.


```
coverage exclude -line 314 -code s -scope
/ethmac_tb/dut/dut/miim1
```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Questa One Sim (ngcoverage) Coverage Migration Guide
Exclusion Commands Migration (Continued)

Branch Exclusions

- No change is required to the exclusion commands. (2025.2)

FSM Exclusions

- No change is required to the exclusion commands.

Expression/Conditions Exclusions

- In some cases, rows order in Expr/Condition tables may differ between next-gen and legacy coverage

Recommendation
Please check the exclusion commands before applying them to make sure that they map to the correct coverage item

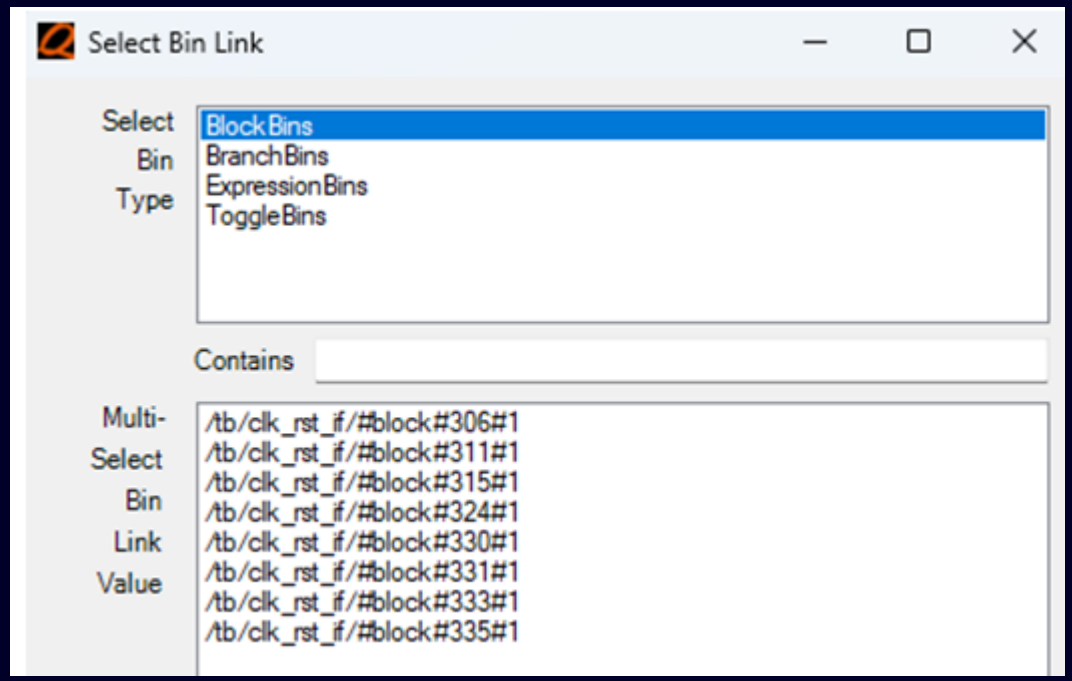
Questa One Sim (ngcoverage) Coverage Migration Guide
Testplans

Testplans Changes

Block Coverage bin links

#stmt# → #block#

Select Bin Link in Questa Excel Add-in will show "BlockBins"



Tag links are unchanged

"-code s"

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Questa One (ngcoverage) Coverage
FAQ

Q?: How will this change my coverage %?

Answer: It can be different. The new percentage number better reflects remaining effort

Comparing coverage % between engines isn't useful information. View this like a different code coverage engine.

Q?: Will I have more bins or less?

Answer: Hard to predict. Blocks are usually less than statement. Toggle are often more.

Constructs off by default remove bins. Likely more bins than coveropt3

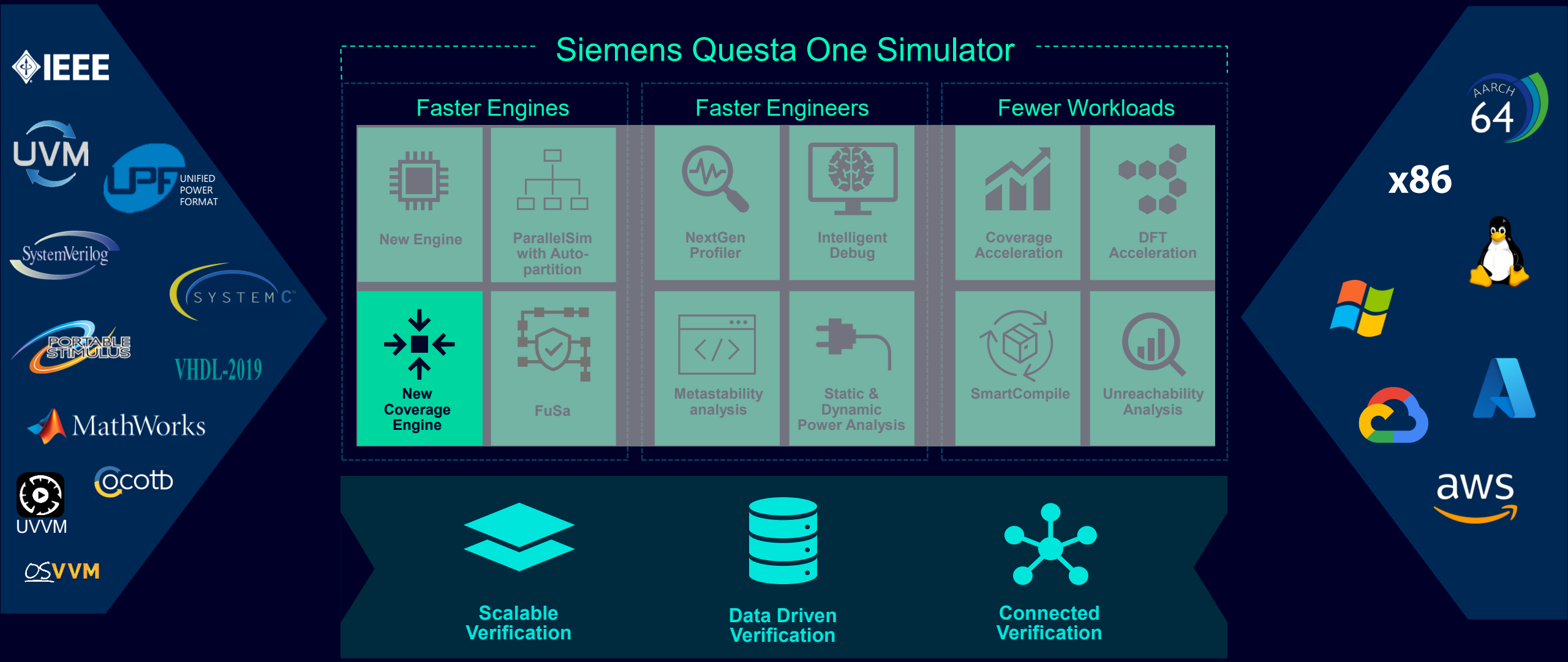
Q?: How much faster will my coverage be?

Answer: 28% on avg

Internal answer: The more optimized full regression, and larger overhead for legacy, the more room for improvement.

Questa One Simulator

Purpose built to meet the productivity demands of the industry



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Siemens Questa One Simulator

Faster Engines

- New Engine
- ParallelSim with Auto-partition
- New Coverage Engine
- FuSa

Faster Engineers

- **NextGen Profiler**
- Intelligent Debug
- Metastability analysis
- Static & Dynamic Power Analysis

Fewer Workloads

- Coverage Acceleration
- DFT Acceleration
- SmartCompile
- Unreachability Analysis

Scalable Verification

Data Driven Verification

Connected Verification

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Use Model Refresh - Data Generation

- qopt/vopt -fprofile[+options]
- qsim/vsim -fprofile[+options][+engine][+testname=<test_name>]

options:

+file=<file_name>	:Write data to the specified fdb
+dir=<dir_name>	:Create fdb files inside <dir_name>
+tag=<string>	:Tag FDB file names with <tag>

engine:

+perf	: performance profiler
+solver	: solver profiler
+mem	: memory profiler
Default	: Usage profiler

testname: ***NEW***

<test_name> identified by the customer, used by multi-test profiler

Use Model Refresh - Data Analysis

- qsim/visualizer [-fbatch] -fprofile [+engine][[+options] | [+compare_options]][+report_options]

options:

+file=<file_name>
+dir=<dir_name>
+tag=<string>

engine

+perf
+solver
+mem
+mass

report_options

+report[=<file>] :Report on all available data trees in a formatted ASCII text report
+data=<search_string> :Filter the generated report by <search_string>
+csv :Print report in csv format

compare_options (Currently supported for usage and performance profiler)

+compare+file1=<fdb1>+file2=<fdb2>

-fbatch

UI is not loaded

Multi-test Profiler Use Model

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Multi-test Profiler
Use Model

- **Data Generation :**

  Same as regular profiler generation

  Performance : vsim/qsim -fprofile+perf
  Solver : vsim/qsim -fprofile+solver [-solverfprof=<options>]

- **Data Analysis :**
  - qsim -fprofile+mass[+engine][+options]
    - engine : +perf , +solver
    - options
      - default ➔ loads all fdbs in fprofile directory
      - **+dir=<>** ➔ provide multiple +dir to load multiple dirs of fdbs
      - **+file=<>** ➔ provide multiple +file to load all specified fdbs

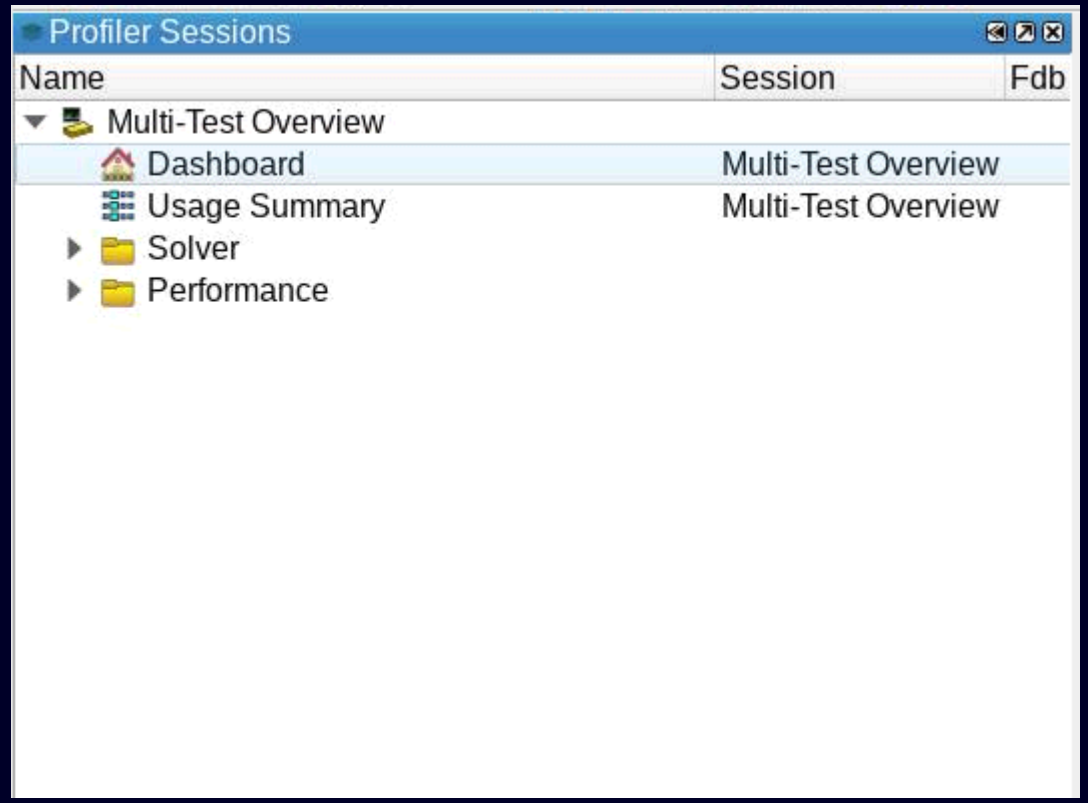
NEW

      - **+filelist=<>** ➔ loads all fdbs specified in filelist
      - **+rdir=<>** ➔ searches and loads all fdbs in provided directory

  - Note:
    - **Fdbs of different version than the 1st fdb will be ignored**

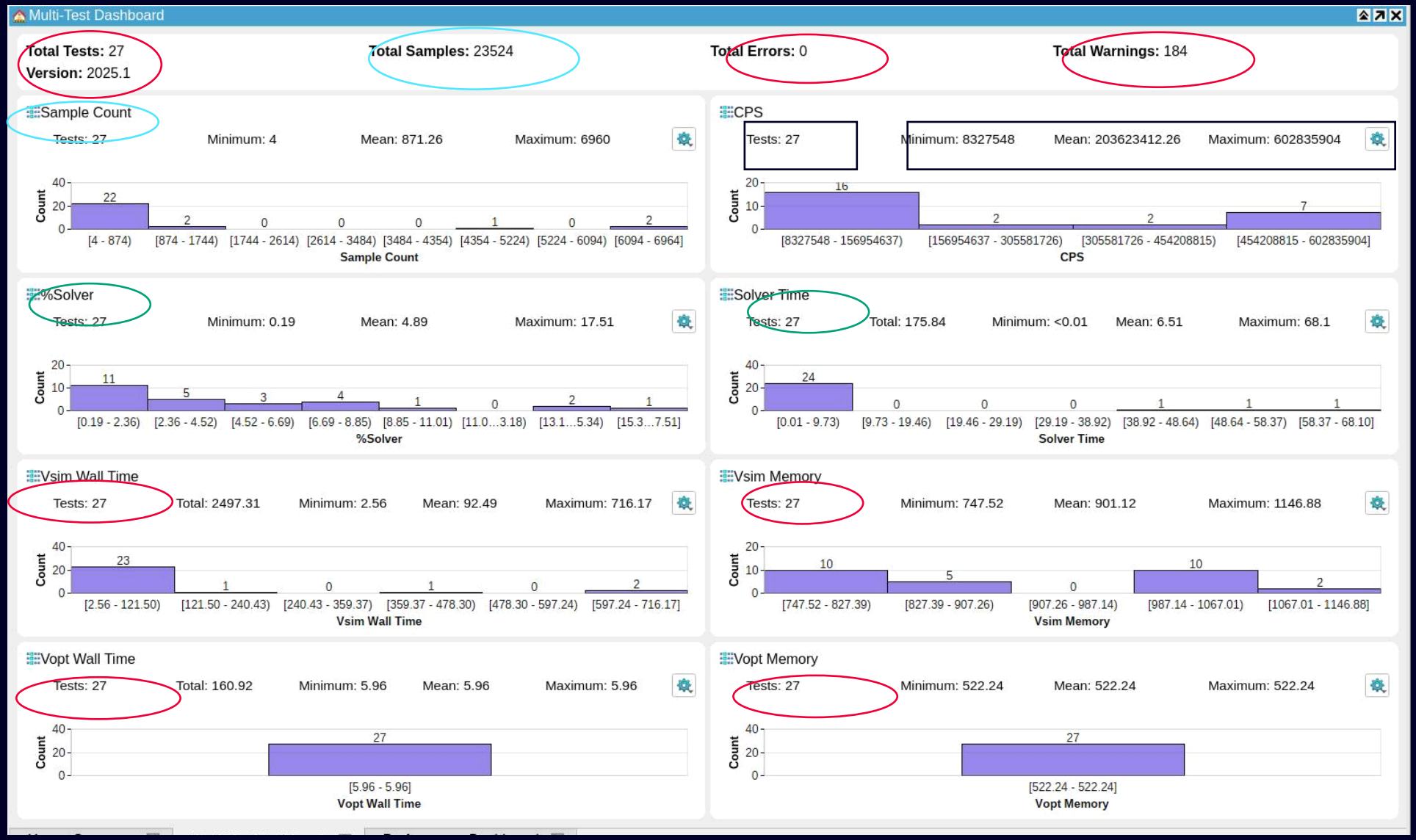
Multi-test Profiler
Supported Clients

- Usage
- Performance
- Solver
- ParallelSim Qualifier



All clients are merged under a single Session

Multi-Test Profiler Windows
Dashboard



Usage (default)
Performance
Solver

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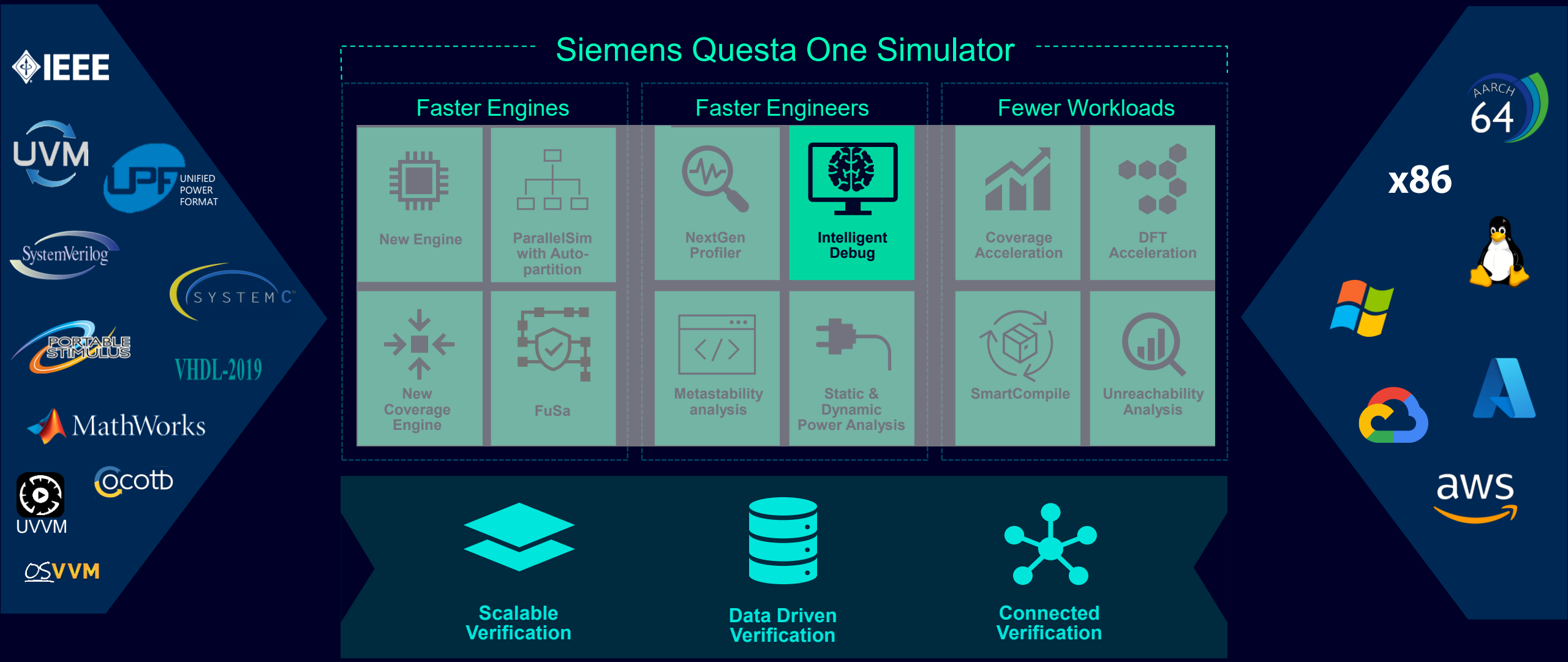

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The most advanced debugger included with every Questa Sim

“Visualizer inside” Siemens Enterprise Verification Platform

On-demand loading

Compact DB
- waves, design, coverage

Unique features
- Multi-test profiler
- Heat-map x-debug
- Interactive coverage analysis

Cool features
- What-if constraint analysis
- Omni-search
- Time Cone
  - X tracing
  - “Any transition” tracing

Best in class UVM Debug
- Schematic
- Class instances
- Classes in the wave window
- Transaction debug
- Interactive debug
  - Sequence Window
  - Breakpoints
    - File/Line, Break-on-Change

Seamless platform integration
- Avery VIP protocol-aware
- Veloce HW/SW debug
- Symphony Pro AMS

FSM Debug

Schematics
- Smart flattening
- Smart pruning

Memory Viewer

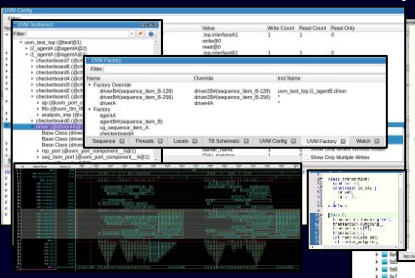
Real number modeling

Power Aware Debug

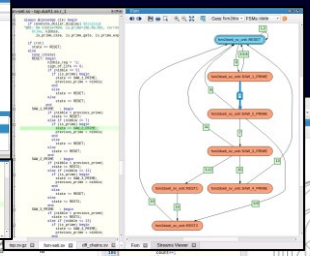
Waves
- Custom Radix
- Biometric Search
- Wave Expressions
- Count Events
- Grid Events
- Markers

More …

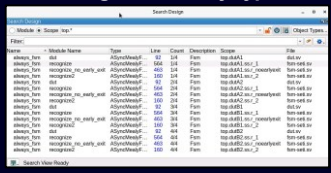
UVM classes and transactions native everywhere

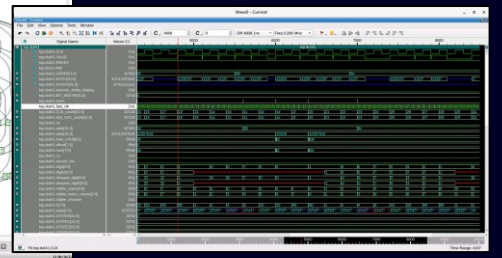


FSM debug & cross probing

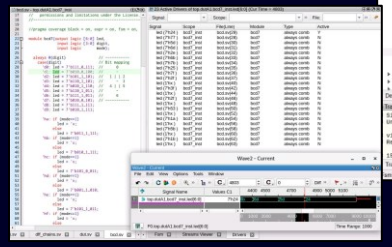


design search by type



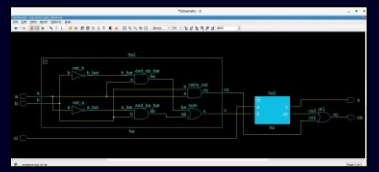


waveforms with cross probing & biometric search

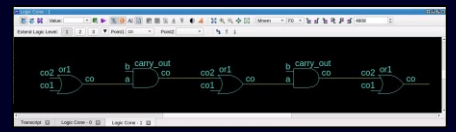


driver/receiver tracing from wave and source code

schematics with smart hierarchical flattening



‘x’ tracing through sequential logic and time



schematic exploration with smart pruning

And even more features with Questa One Sim!

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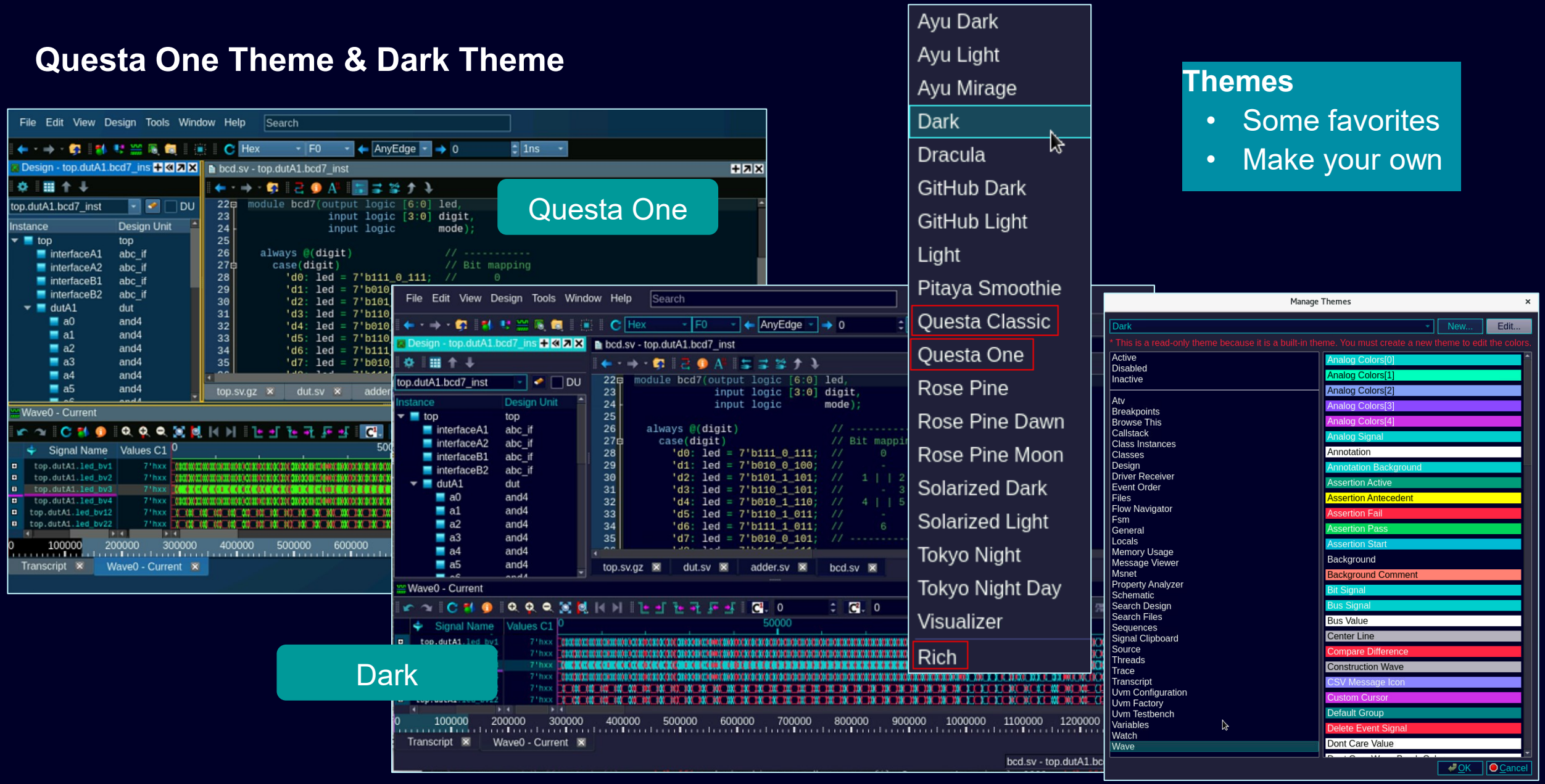
Questa One Theme & Dark Theme



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Dragging Windows

Infinite drop locations

Drag the Tab “header” → Turns into a “managed window”

Drag the managed window frame… It stays “not dropped in”

Drag the tab header in the managed window to “drop the tab in somewhere”

Buttons, stdio reading, tcl commands, scripting…

VHDL stdin reading

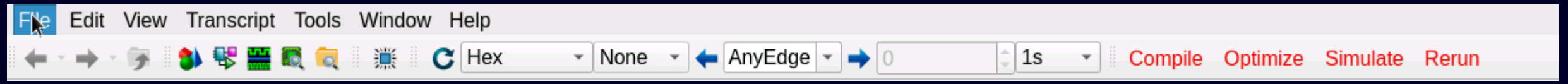
gets stdin

Tcl command support - ~389 with many switches

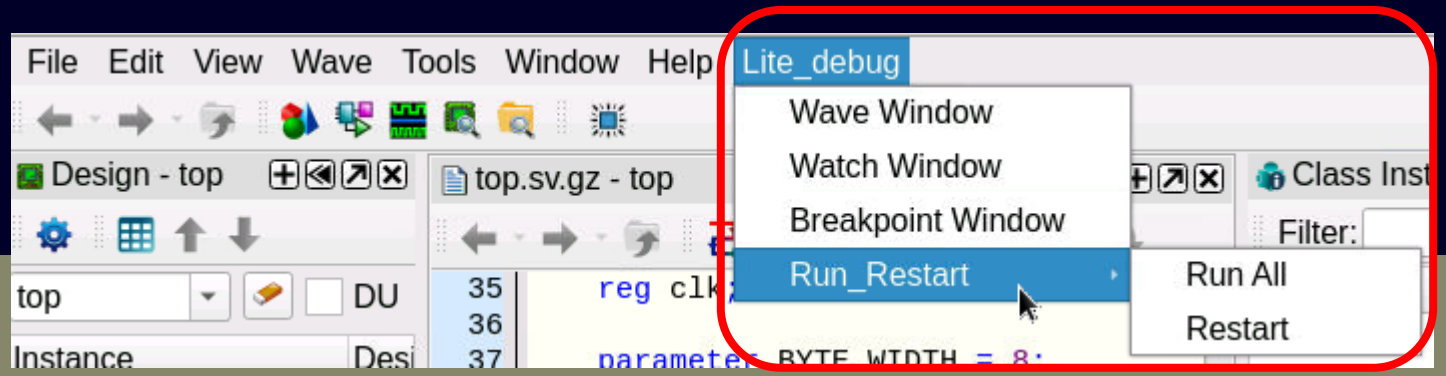
Users can use existing scripts

Buttons / Menus / Toolbars

```
add button Compile  {do compile.do}  NoDisable {-fg red -bg pink}
add button Optimize {do optimize.do} NoDisable {-fg red -bg pink}
add button Simulate {do simulate.do} NoDisable {-fg red -bg pink}
add button Rerun    {do change.do}   NoDisable {-fg red -bg pink}
```



Buttons and Menus




```
set myglobalvar 0

proc AddMyBtn {wname} {

  global myglobalvar
  set cmd1 "echo Wave!;   view wave $wname"
  set cmd2 "echo Watch!;  view watch $wname"
  set cmd3 "echo BP!;     view breakpoints $wname"
  set cmd4 "echo Run All; run -all $wname"
  set cmd5 "echo Restart; restart $wname"

  add_menu       $wname Lite_debug
  add_menuitem   $wname Lite_debug              "Wave Window"       $cmd1
  add_menuitem   $wname Lite_debug              "Watch Window"      $cmd2
  add_menuitem   $wname Lite_debug              "Breakpoint Window" $cmd3
  add_submenu    $wname Lite_debug              Run_Restart
  add_menuitem   $wname Lite_debug.Run_Restart  "Run All"           $cmd4
  add_menuitem   $wname Lite_debug.Run_Restart  "Restart"           $cmd5  -variable myglobalvar  \
                                                                           -onvalue 1 -offvalue 0  -indicatoron 1
}

AddMyBtn  $wname
```

Omnisearch Demo

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X-Debug

Sources of Xs

- How are X-values generated in simulation?

Assigned X-values	• Assigned by designers under conditions which should not occur • Default case statements
Uninitialized State Elements	• Uninitialized state elements/registers are Xs • Incomplete reset operation • Power Aware Simulation produces X values
Secondary Sources	• Bus conflicts/multiple drivers • Out-of-range index • Incorrect arithmetic (divide by zero)

Siemens Solution

Static Solutions

- Exhaustively identifies all X-state issues
- Enables exhaustive evaluation of circuit start-up and post-reset “X” issues
- Static Products includes Questa Lint, Questa Inspect, Questa Xcheck, Questa CDC/RDC/Simulate FX

Dynamic Solution for RTL

- Ensures simulation closely matches the silicon behavior
- Traps the source of X during simulation
- Ensures signals resolve to a known value if possible
- Dynamic Solution for RTL - QuestaSim

Dynamic Solution for Netlist

- For Gate level Simulation X-pessimism
- Eliminates false Xs automatically
- Eliminates zero-delay race conditions
- Eliminates library modelling error
- Finds and corrects any X-pessimism found on a path
- Dynamic Solution for Netlist- SimXACT

Questa X verification solutions eliminate X-related issues, and more

Eliminating issues and improving design quality from creation through completion

X Solution	Benefits	Limitations
Questa Lint	➢ Run early and often ➢ Minimize X sources as early as possible ➢ Minimize bugs	No support for sequential related X sources
Questa Inspect	➢ Minimize X sources ➢ Correct initialization issues ➢ Find complex corner case bugs	No support for corruption due to X-propagation
Questa Check X	➢ Remove random design behavior due to unexpected X-propagation ➢ Minimize flops needing resets	No support for verifying design behavior
CDC/RDC Simulate FX	➢ Unmask problematic structures early. ➢ Comprehensive coverage of domain crossings and clock-reset tree	Targets domain crossing paths and clock-reset tree only

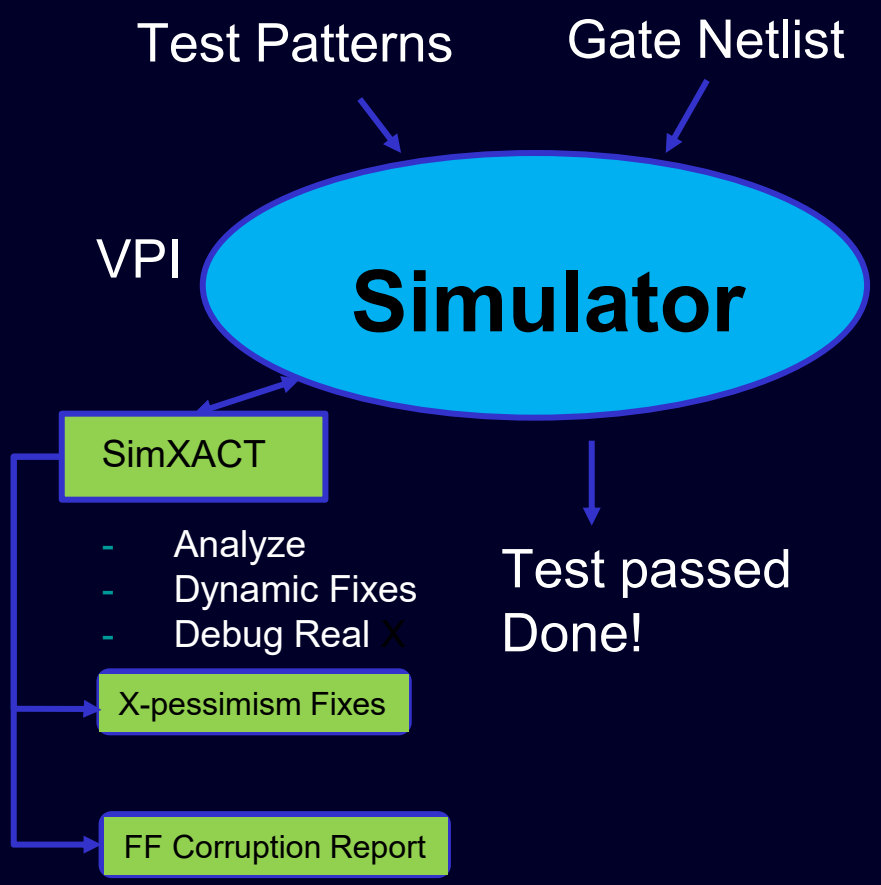
Questa X verification solutions eliminate X-related issues, and more

Eliminating issues and improving design quality from creation through completion

X Solution	Benefits	Limitations
Questa Simulation **XProp**	➢ Unmask initialization related bugs ➢ Better correlation between RTL and gate sims	May increase simulation time
SimXACT	➢ Remove FalseX (X-Pessimism) by analyzing and providing fix for FalseX. ➢ Work only on Gate level Netlist	Analysis time during Gate level Simulation is significant but it reduces overall debug time, eliminating all FalseX

Part Of Questa One

SimXACT Flow for Gate Simulation



SimXACT is a 3rd party VPI program to be run with simulator. All analysis is formal and performed under the hood.

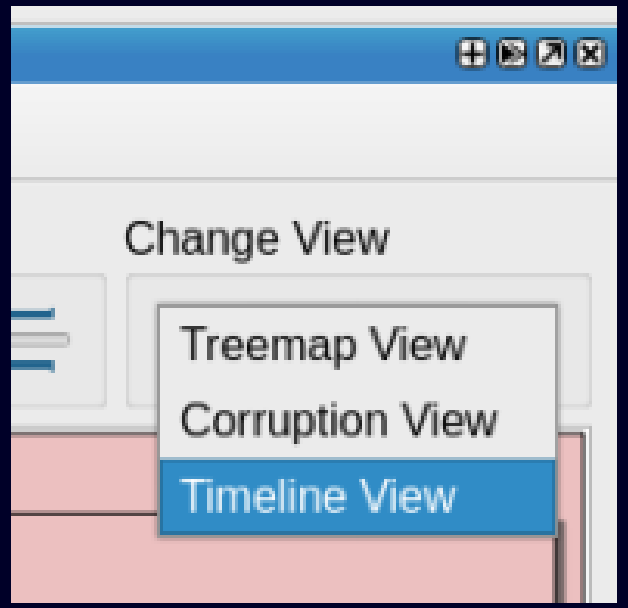
- SimXACT eliminates all false Xs and real Xs still propagate out
  - If a test passed, the original failure was due to false X and is not a real issue!
  - If a test failed, because all false Xs are cleaned, debugging Xs becomes much easier
- SimXACT also writes out X-pessimism fixes for further simulation as well as FF corruption report for X debugging.

SimXACT: Use Model Change – New Flow (contd..)

- New Flow
  - ❑ Find false Xs
    - ✓ qopt **-simxact_findx**
    - ✓ qsim **-simxact_findx[=simxact_dut=dut_location][,simxact_delay=start_time_in_ns][,simxact_config_file=fileName][,incremental]**
  - ❑ Apply fixs
    - ✓ qsim **-simxact_applyfix**
  - ❑ Merging fixes
    - ✓ qsim **-simxact_findx=incremental**

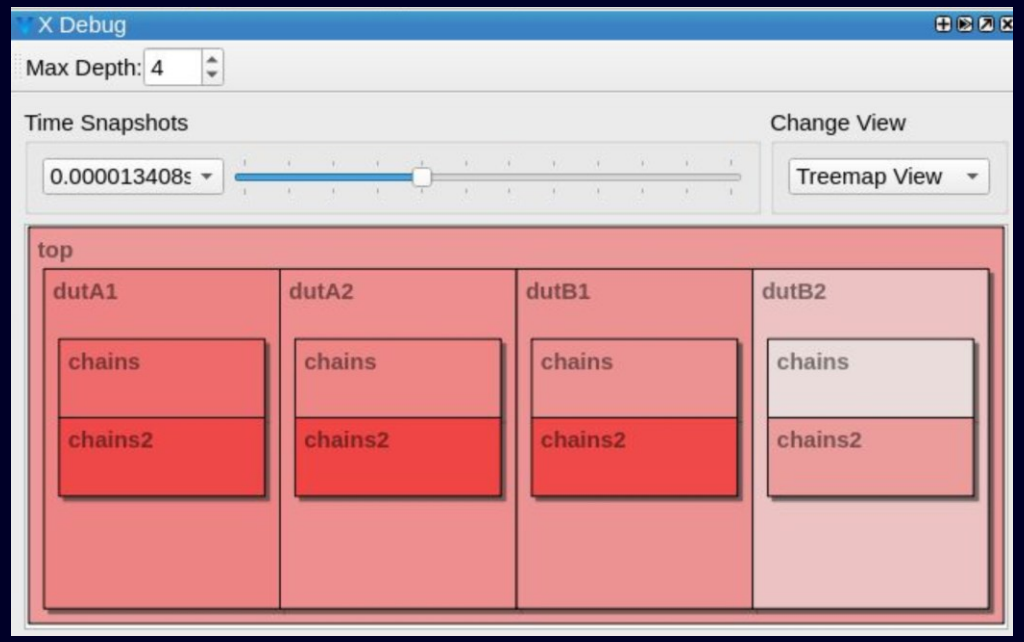
SimXACT: Integration with Visualizer

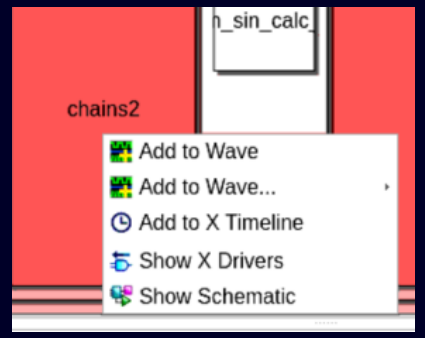
- It's a visualizer window that mainly displays the distribution of X values within the module and submodules of the design.
- Completely independent feature for debugging Xs. It can be used with or without SimXACT (findx/applyfix).
- XVISDB_DUMP can be used in both RTL and gate level simulation
- X-Debug has 4 main views:
  - Treemap view
  - Corruption view
  - X Timeline view
  - X Drivers view



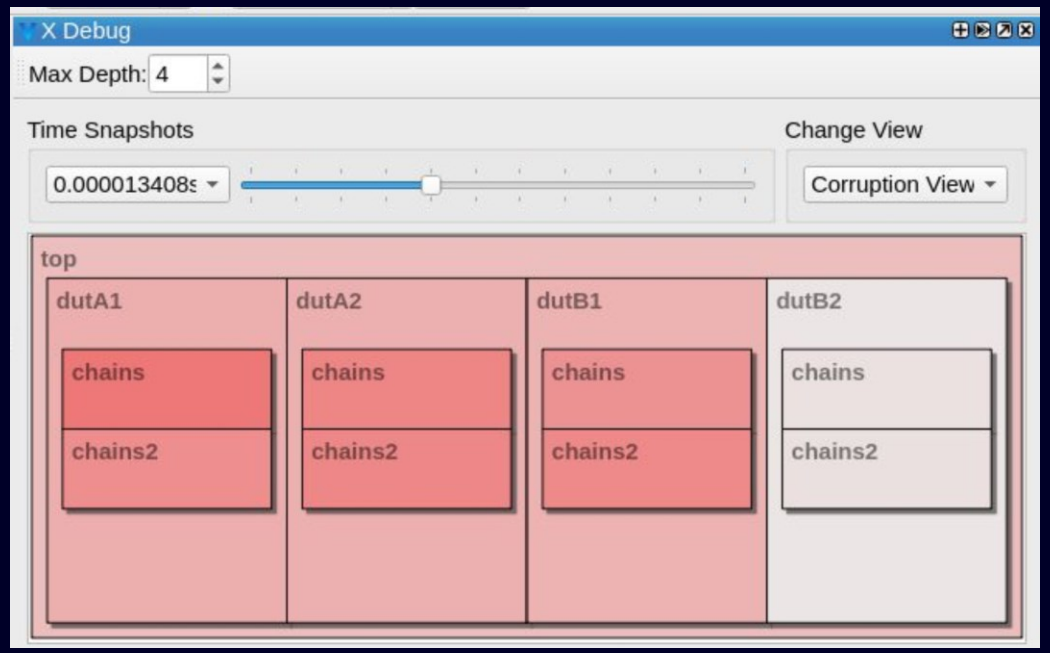
SimXACT: Xdebug – Treemap view & Corruption view

- Treemap view





- Corruption view



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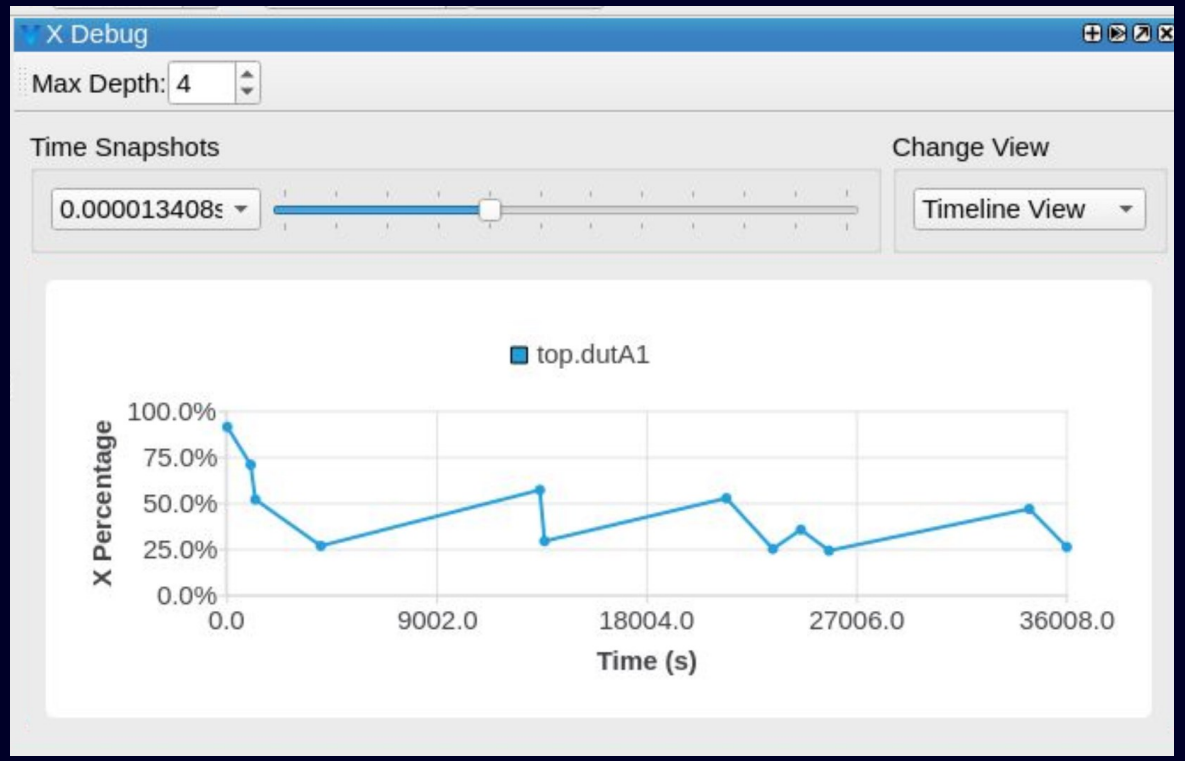
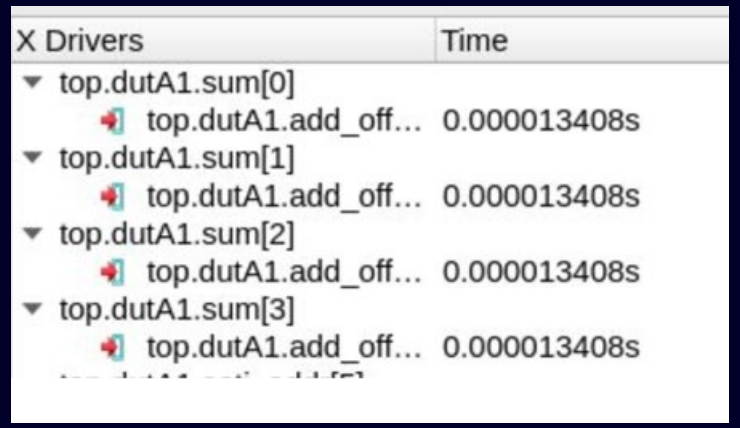
SimXACT: Xdebug – X Timeline view & X Drivers view

- X Timeline view



- X Drivers view



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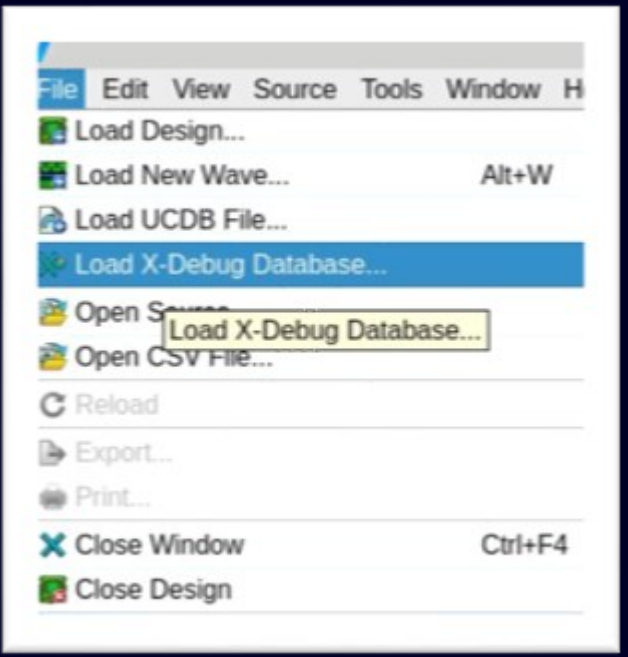
SimXACT: X Debug (contd..)

- Generating an X Debug database:
  - Add option qopt -xdebug_dump
  - Add option qsim -xdebug_dump=+file=filename+dut=dut_name+interval=interval+x_change=change+type=auto,ff,output,reg,var,net
  - Loading XDebug database in visualizer:
  - visualizer design.bin +xdebugdb=xdebug.xdb +q1xdebug



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Constraint Debug

Constraint Debug – Use Model

Available in Live sim mode in Questa One Sim only

Use Model

- vlog test.sv
- qopt **-debug -designfile design.bin** top -o opt
- qsim **design.bin** opt **-qwavedb**=+signal+class+**constraint_debug**+…
- Add Randomize breakpoint
- Run
- View -> Constraint Debug

Randomize Breakpoints

Available on randomize calls:

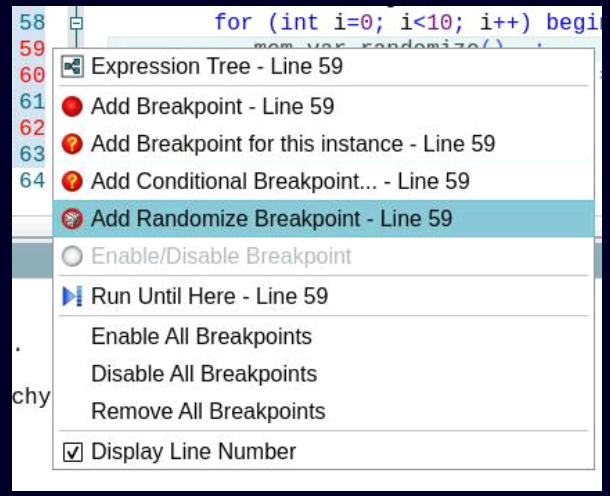
1. From src window
2. From Classes window
3. From Class Instances window

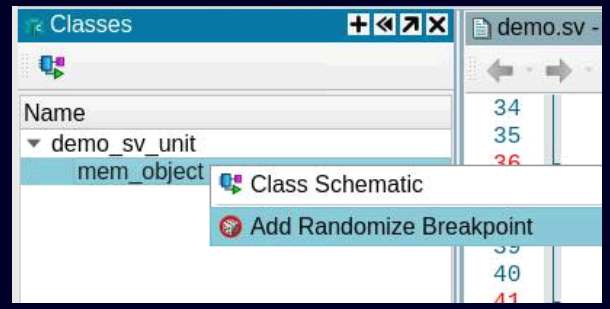
4. Tcl command

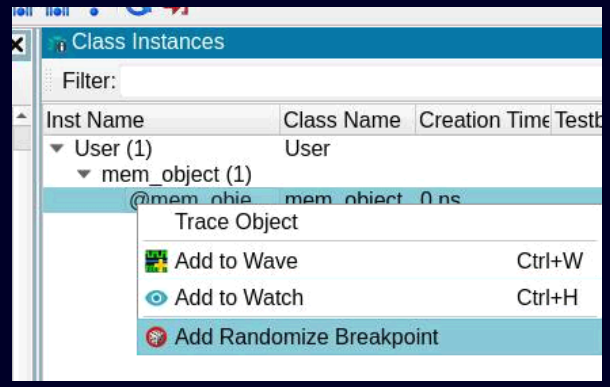
   bp -randomize <src_file> <line_number>

   bp -randomize -class <class_name>

   bp -randomize -class_instance <class_instance>







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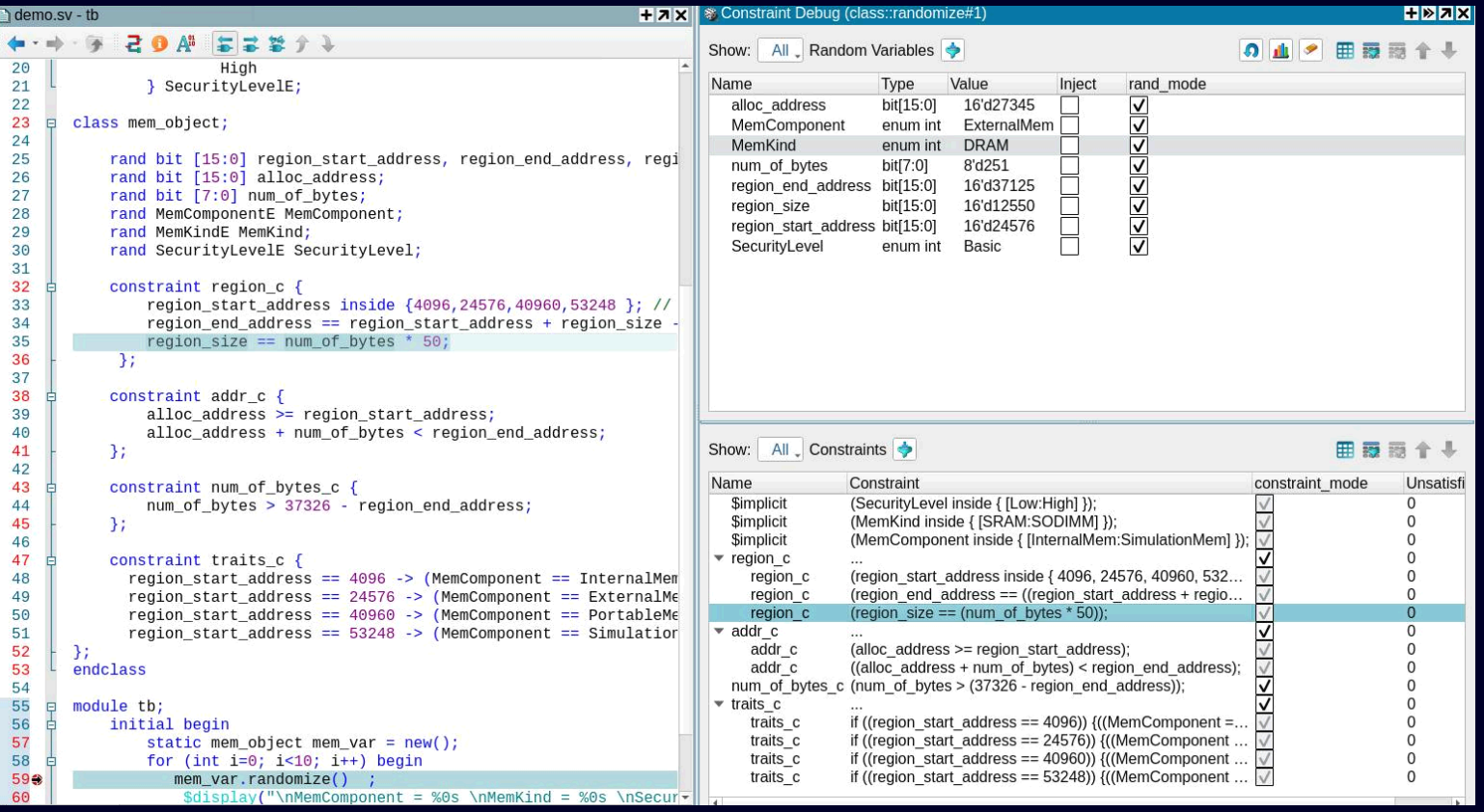
Constraint Debug Window



Random Variables Pane

Constraints Pane

- Recent Changes
  - Type matches the variables window type
  - Changing Radix
  - Constraints hierarchal representation

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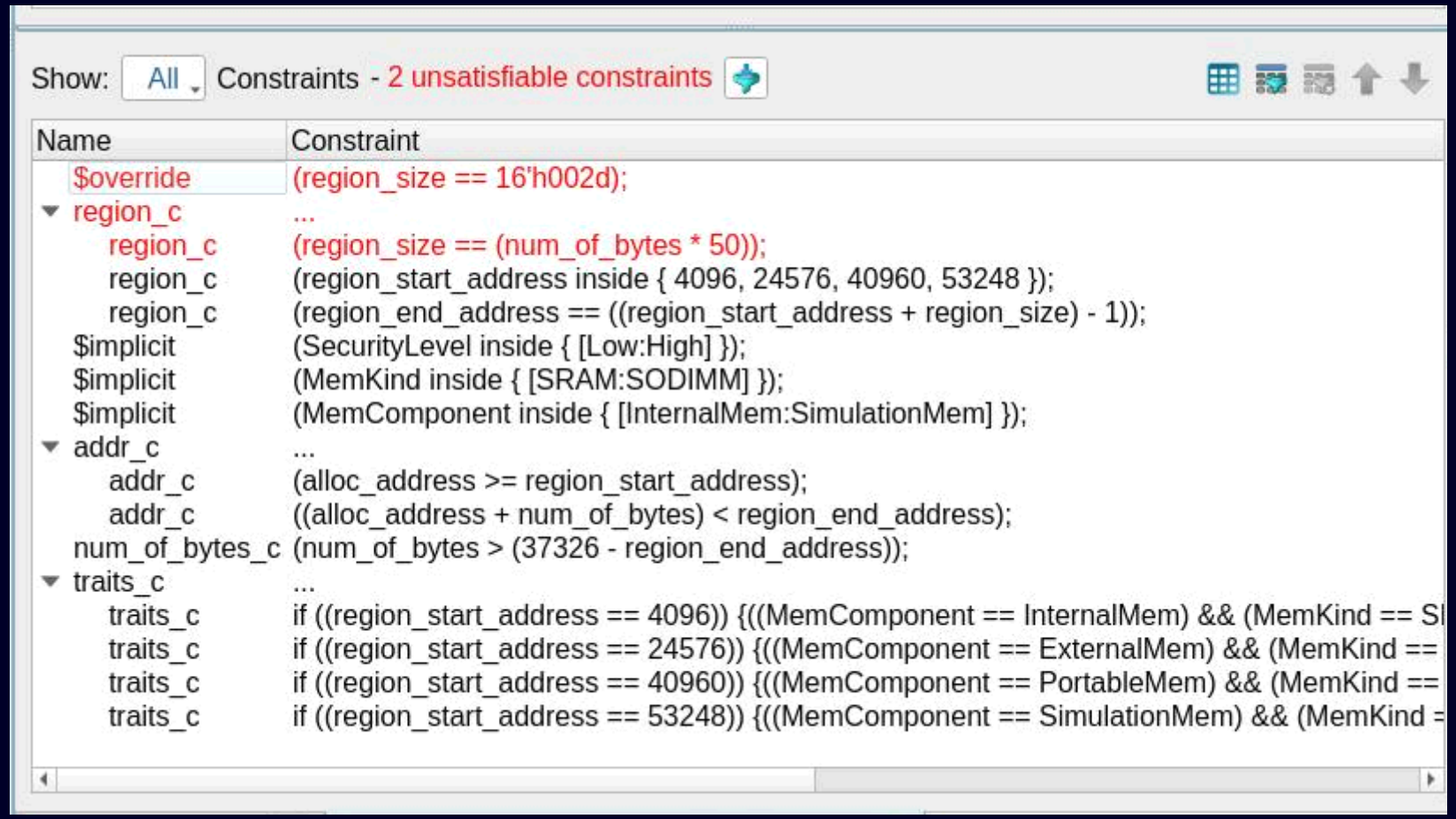
Constraint Debug Window
Constraints Pane - Conflicting Constraints



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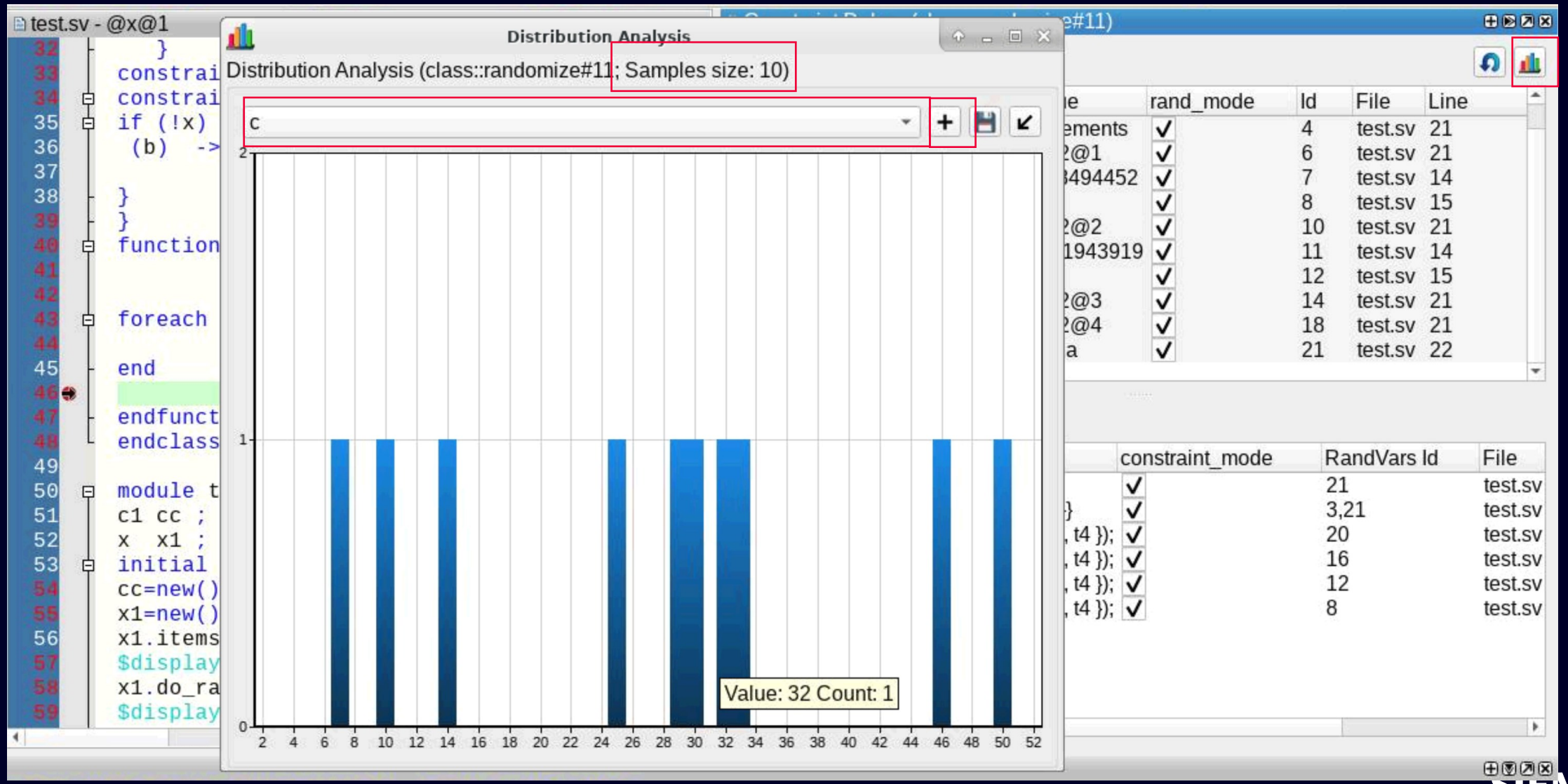
Constraint Debug Window
Distribution Analysis



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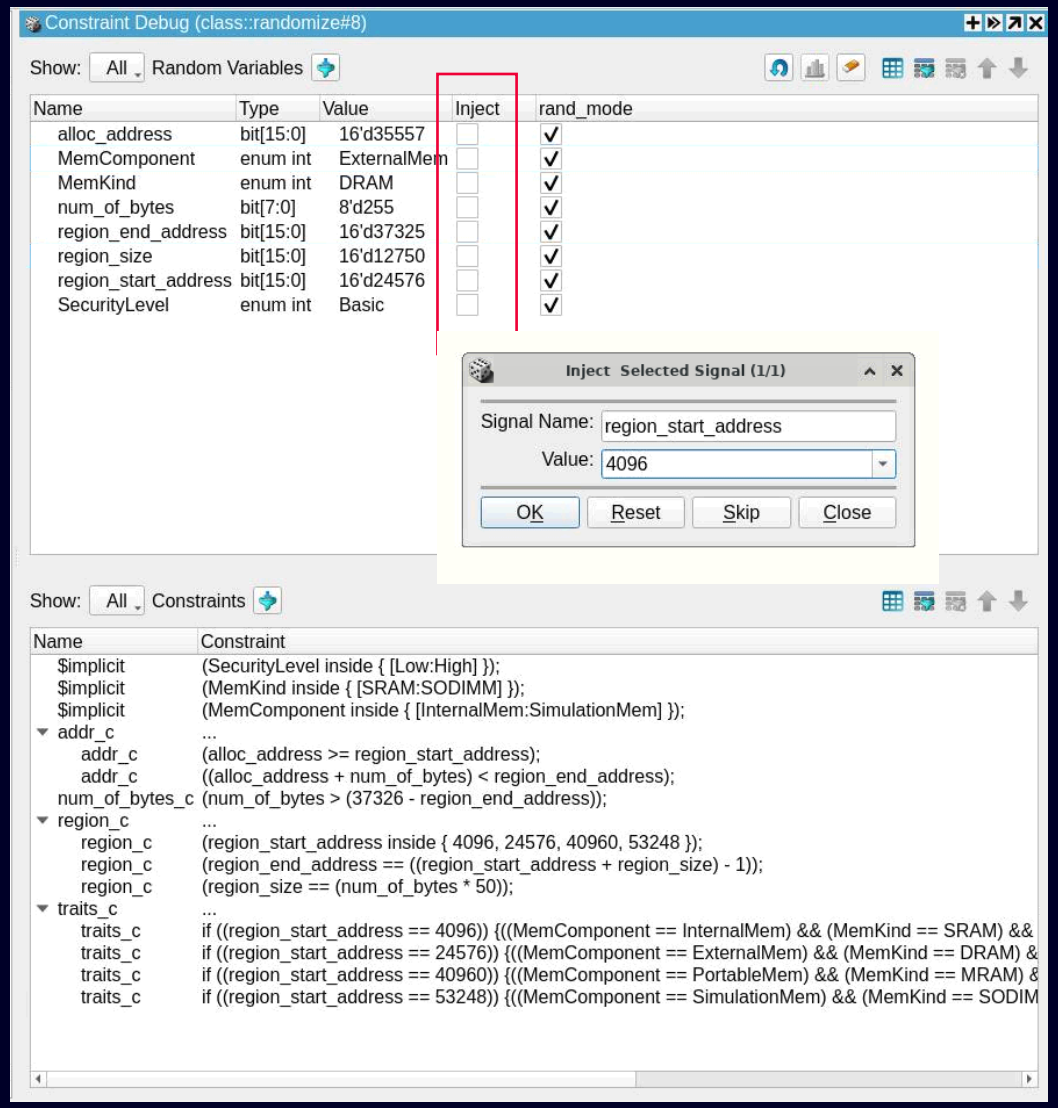
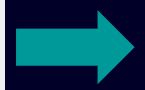
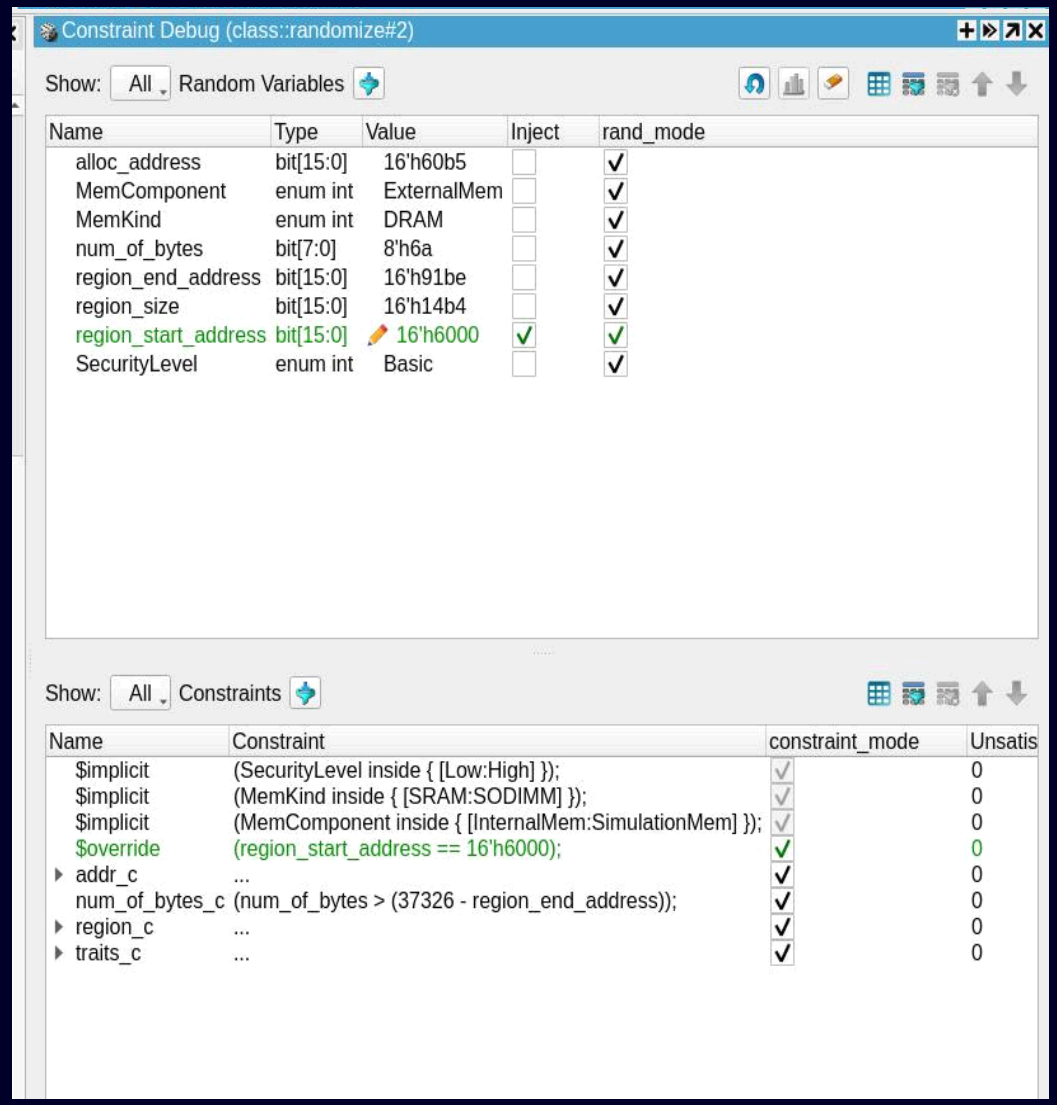
What if Analysis







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2025 upcoming and on-demand webinars

https://eda.sw.siemens.com/en-US/eda-events/

20
Webinars

Unlocking the Power of QuestaSim and Visualizer Integration

PCIe Gen7 Verification with Siemens Avery Verification IP

Faster Debug of Complex Testbenches using Visualizer

Breaking Barriers: Ethernet 1.6T, Infiniband, UALink, and UEC Verification for Next-Gen Connectivity

Explore How to Protect Against Data Corruption with Formal Security Verification

Smart Debug: Accelerate Root Cause Analysis and Reduce Debug Turnaround Time with Questa Verification IQ Regression Navigator

An End-to-End Functional Safety Solution for Automotive ICs Based on ISO 26262

Improving FPGA Safety and Security Compliance: FPGA Equivalence Checking to the Bitstream

Faster Debug Using QuestaSim Interactive Coverage Analysis

Streamlining FPU Verification with an Alternative to C-reference Model Approaches

Smart Regression: Optimize Regression Efficiency Using Questa Verification IQ Regression Navigator

In this webinar, we explore the powerful smart regression features of collaborative browser-based data-driven verification. You will then learn how to harness the full potential of Questa Verification IQ to boost efficiency and productivity in your verification efforts, take advantage of

Securing your FPGA Design from RTL through to the Bitstream

This session will briefly introduce practical tools such as the Siemens Analyze Architecture and VerifySecure technologies, highlighting how they support the overall security strategy. In addition, we will introduce

Solving the Semiconductor Verification Crisis: From Problem to Productivity

Wednesday, May 21, 2025 | 8:00 AM Pacific Daylight Time | 1 hour

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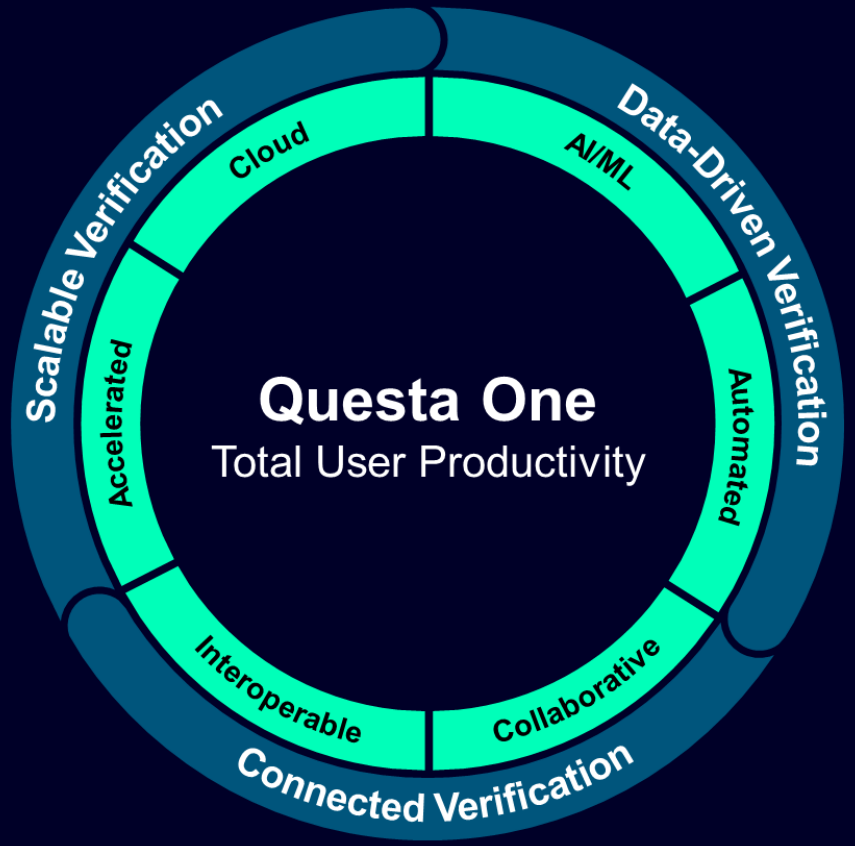
Questa One – Next Generation of Smart Verification Solution enabled by AI
Improving user productivity through the collective power of technology



Faster Engines ▲

Faster Engineers ▲

Fewer Workloads ▲

Delivering up to **5x** improved
Total User Productivity

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Questions?

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