

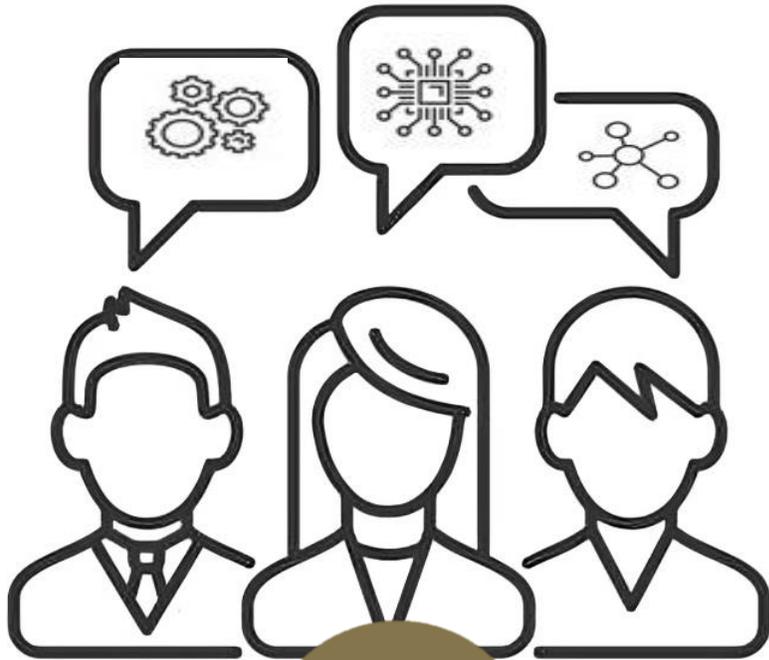
# Capital System Introduction

Topic

- 1 Siemens System Engineering
- 2 Capital System Overview
- 3 Demo – TC import
- 4 Demo – Capital System Modeler
- 5 Demo – Capital System Architecture
- 6 Capital System to Logic
  - ICD flow
  - Generative flow

Closure and Q&A

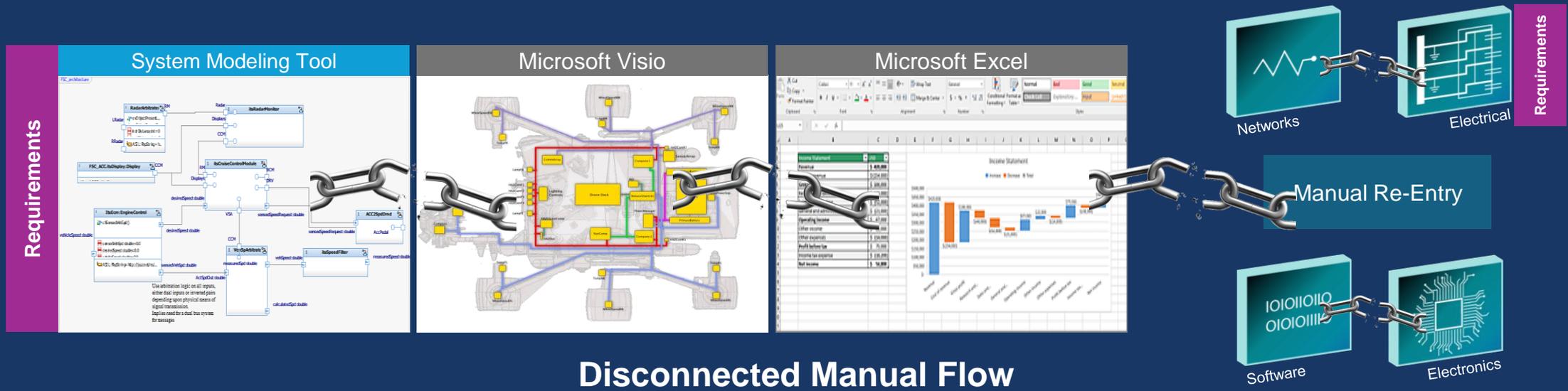
# Why Systems Engineering?



SYSTEMS  
ENGINEERING

- **Facilitates coordination and collaboration**
- **Enhances system reliability, performance, and safety**
- **Optimizes resource allocation and reduces development costs**
- **Supports system evolution and adaptability**

# How is it Done Today?



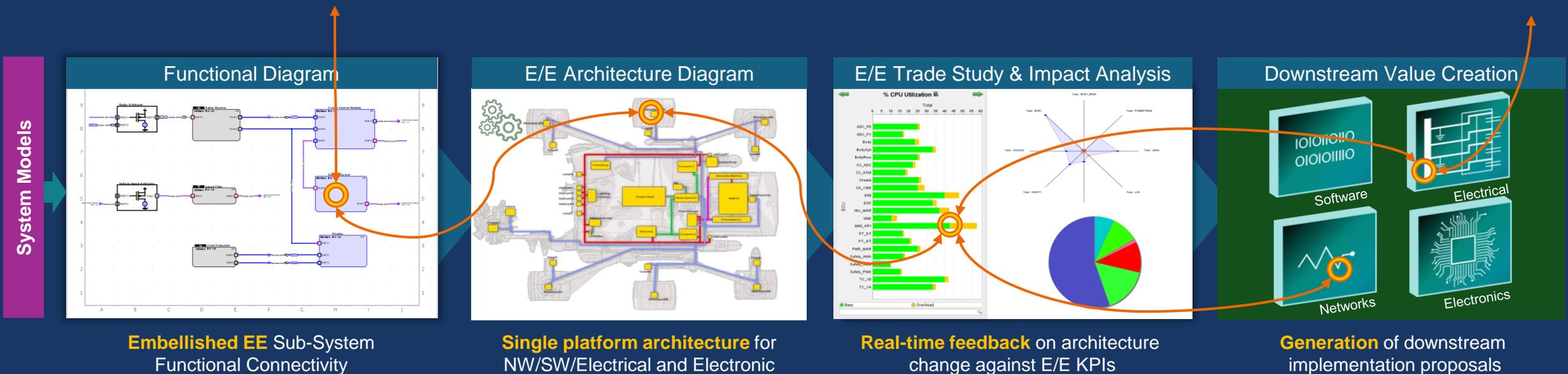
## Disconnected Manual Flow

- **No System Virtual Integration**
- **No Connection to Implementation**
- **Repeat Manual Steps For Each Change**
- **Limited reuse of data**

# Model-Based E/E Architecture

## Integration and deployment of system content into an E/E platform

### Requirements



# Model Based Systems Engineering – MBSE

## Sets up & verify models & requirements for downstream consumption

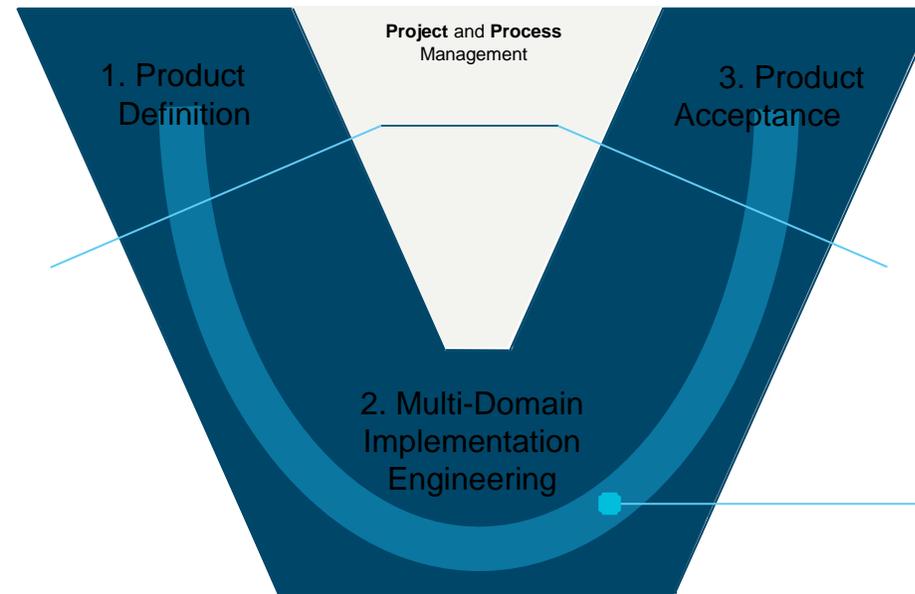
### Model-based systems engineering (MBSE)

is a methodology focused on creating and exploiting domain models for information exchange between engineers

### Product Life Cycle (PLM)

tools provide project and process management throughout as one of its functions

The **System V** is widely used to represent the process flow across model based engineering flows and can be divided into **three primary areas**



A **digital thread** must connect both all sequential elements of the flow as products mature from concept to utilization **and** between collaborating domains maturing in parallel

# Model Based Systems Engineering – MBSE

## Sets up & verify models & requirements for downstream consumption

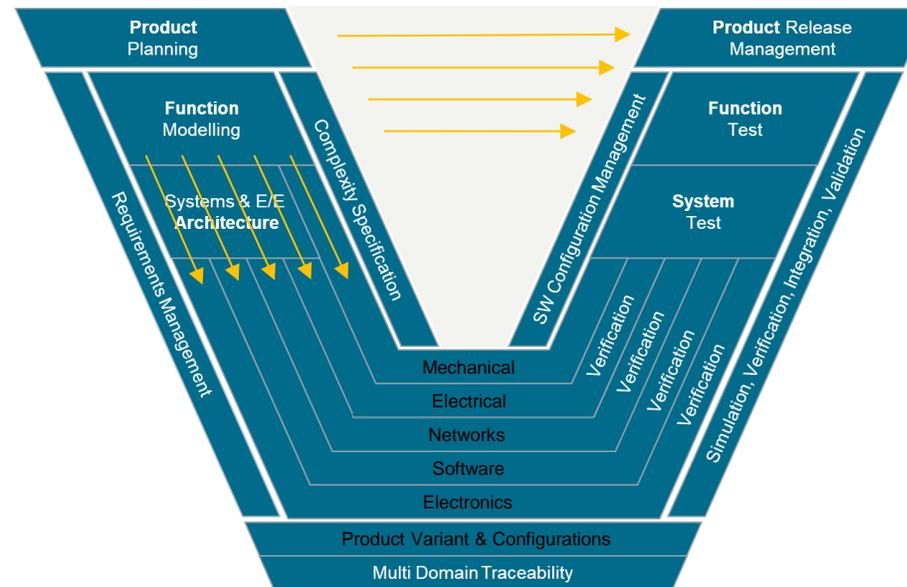
### Model-based systems engineering (MBSE)

is a methodology focused on creating and exploiting domain models for information exchange between engineers

### Capture requirements and create functional models for every included system

- Fn & non-Fn requirements for both hardware and software components
- Author/architect systems models in preferred system engineering tool e.g. SysML
- Manage configurations and resultant BOMs. Orchestrate projects & processes

### Feed verified implementation proposals downstream & simulate against requirements

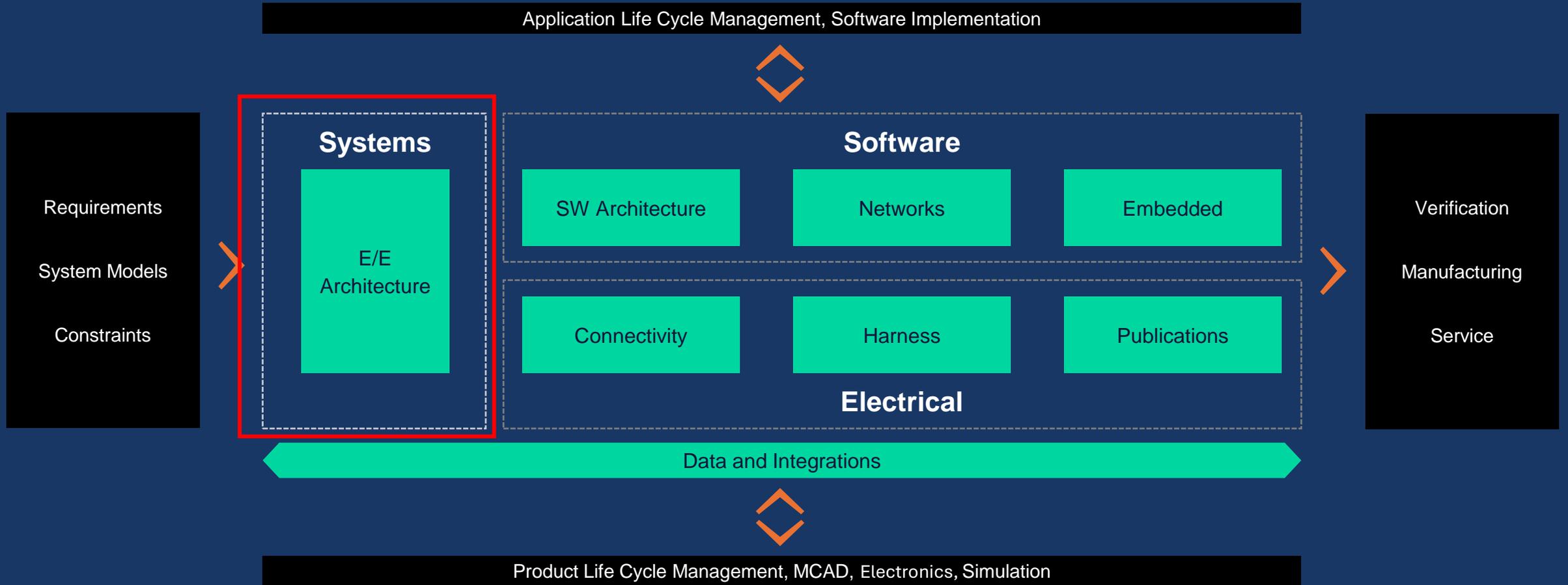


Product Lifecycle Management - PLM

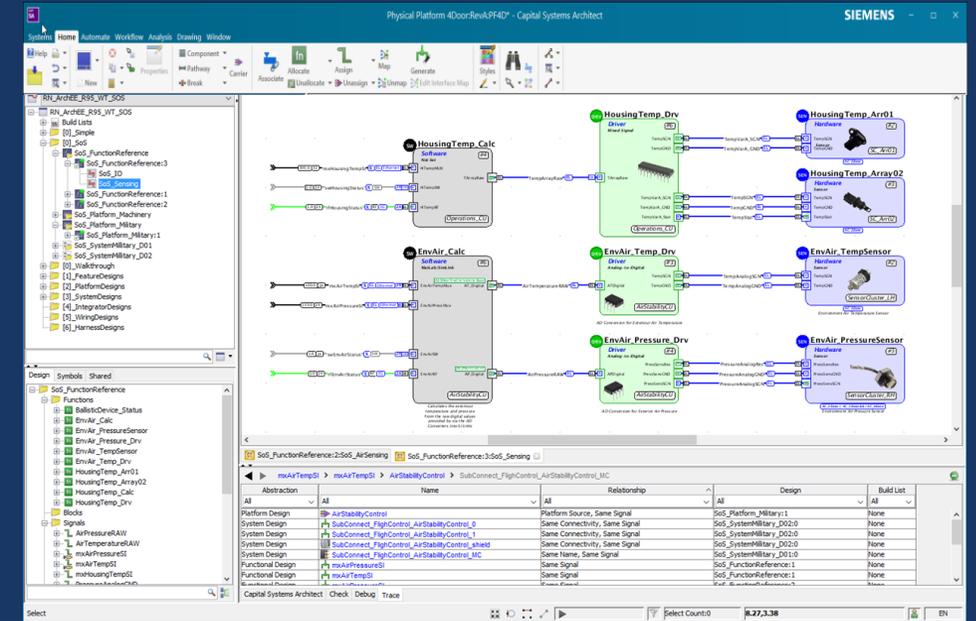
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Closure and Q&A



# Capital Systems Capture Capture & Embellish Functional Designs



- Import functional designs from external sources (examples: SysML, UML) or capture directly
- Capture implementation detail (examples: HW/SW, resource consumption, thermal footprint)
  - Previous projects (carryover) usually provide rich implementation data
- Style diagrams to support preferences of different user communities
- Store data formally as digital twin

# Capital Systems Modeler Function Design Example & Traceability across Abstractions

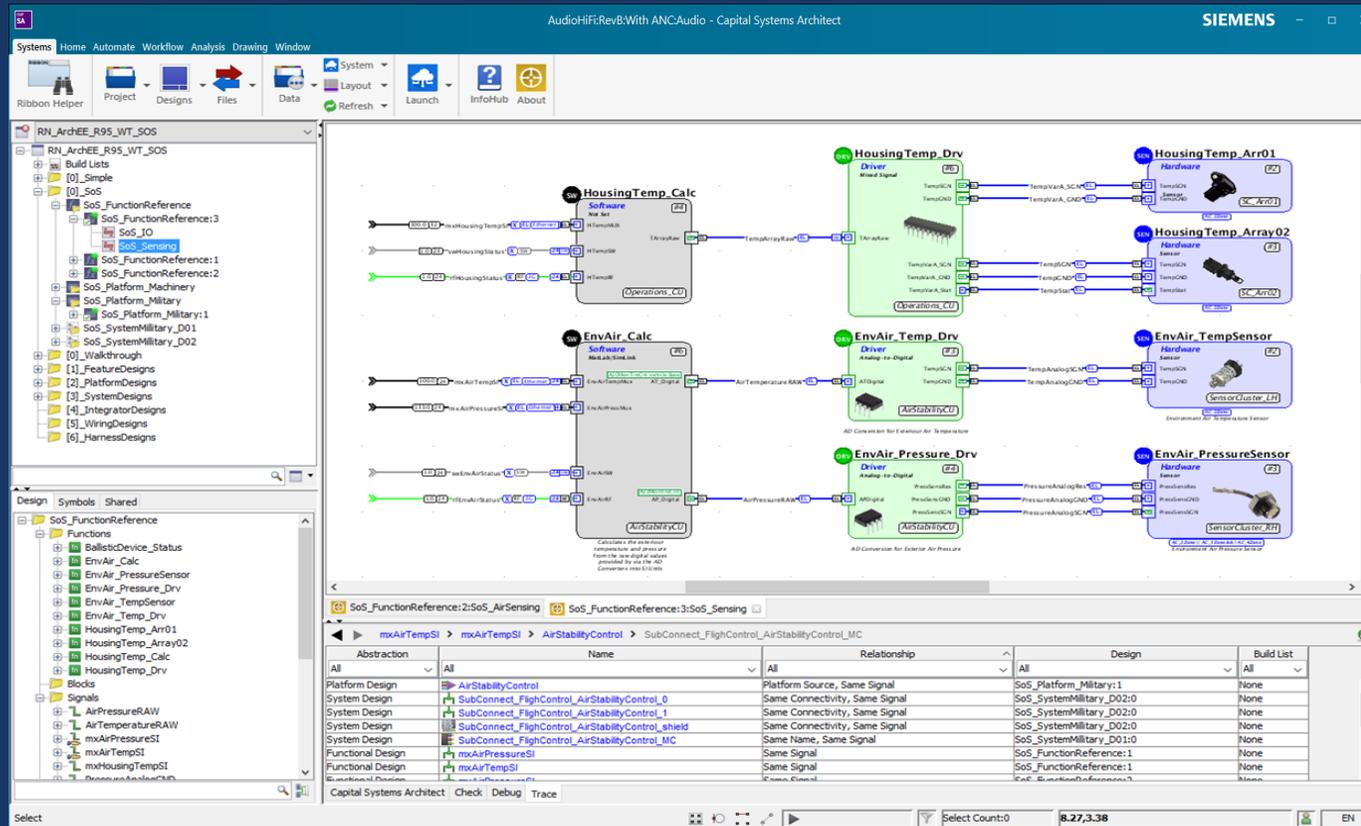
MAY 28<sup>th</sup>

- HW Functions
- Driver Function
- SW Function
- Shared Signals
- Function Design
- Trace & Navigate
- Functions
- Reference Blocks
- Function Signals

Abstraction	Name	Relationship	Design	Build List
Platform Design	AirStabilityControl	Platform Source, Same Signal	SoS_Platform_Military:1	None
System Design	SubConnect_FlighControl_AirStabilityControl_0	Same Connectivity, Same Signal	SoS_SystemMilitary_D02:0	None
System Design	SubConnect_FlighControl_AirStabilityControl_1	Same Connectivity, Same Signal	SoS_SystemMilitary_D02:0	None
System Design	SubConnect_FlighControl_AirStabilityControl_shield	Same Connectivity, Same Signal	SoS_SystemMilitary_D02:0	None
System Design	SubConnect_FlighControl_AirStabilityControl_MC	Same Name, Same Signal	SoS_SystemMilitary_D01:0	None
Functional Design	mxAirPressureSI	Same Signal	SoS_FunctionReference:1	None
Functional Design	mxAirTempSI	Same Signal	SoS_FunctionReference:1	None
Functional Design	mxAirPressureSI	Same Signal	SoS_FunctionReference:2	None

# Enrich and Validate Functional Designs Capital System Modeler

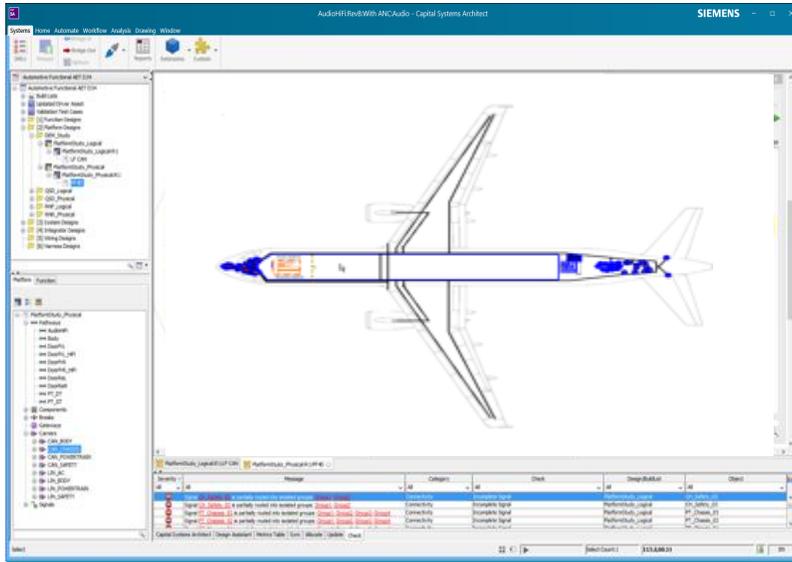
MAY 28<sup>th</sup>



- Break complex systems into subsystems and functions
- Import and normalize functional designs from external sources (examples: SysML, UML) or capture directly
- Capture implementation detail (examples: HW/SW, resource consumption, thermal footprint)
- Enrich functional system models: Network Signals, Electrical Signals, Hardware, Power distribution

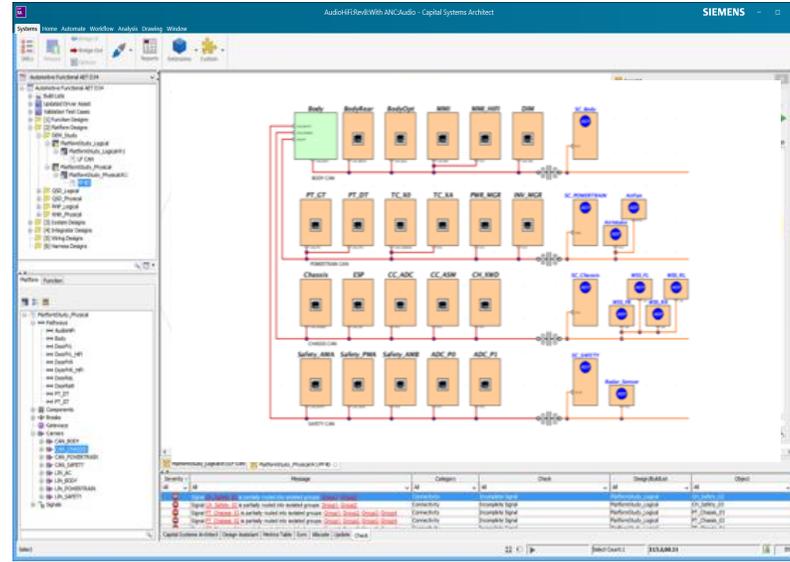
# Capital Systems Architecture

## Capture Topology; Allocate Functions & Signals To Resources



### Physical Platform

*Up-To-Scale Model of Physical Topology*



### Logical Platform

*Hierarchical Network & SW Domain Architecture*

**Constraint Selection** [X]

- [-] Allocation
  - [-] Allocate by Attribute/Property
  - [-] Option Allocate by Attribute/Property
- [-] Attributes and Properties
  - [-] Device Pin Specification
  - [-] Device Specification
  - [-] Message Conductor Specification
  - [-] Signal Conductor Specification
- [-] Mapping
  - [-] Map Signal/Message to Carrier and to Interface by Attribute/Property
  - [-] Map Signal/Message to Discrete Carrier and to Interface by Attribute/Property
  - [-] Map Signal/Message to Interface by Attribute/Property

**Component: POWERTRAIN** [X]

General Graphical Properties Rules

Component: POWERTRAIN (6)

- ✗ Component - ECU - Allocation Constraints
- ✗ Do allocate functions with attribute/property matching *Name = AirFanControl\_D.\**
- ✗ Do allocate functions with attribute/property matching *Name = AirIntake\_D.\**
- ✗ Do allocate functions with attribute/property matching *Name = Component Name*
- ✗ Don't allocate functions with attribute/property matching *Sectional Area <= 15.00*
- ✗ Don't allocate functions with attribute/property matching *Thermal Output >= 90*

Diagram (1)

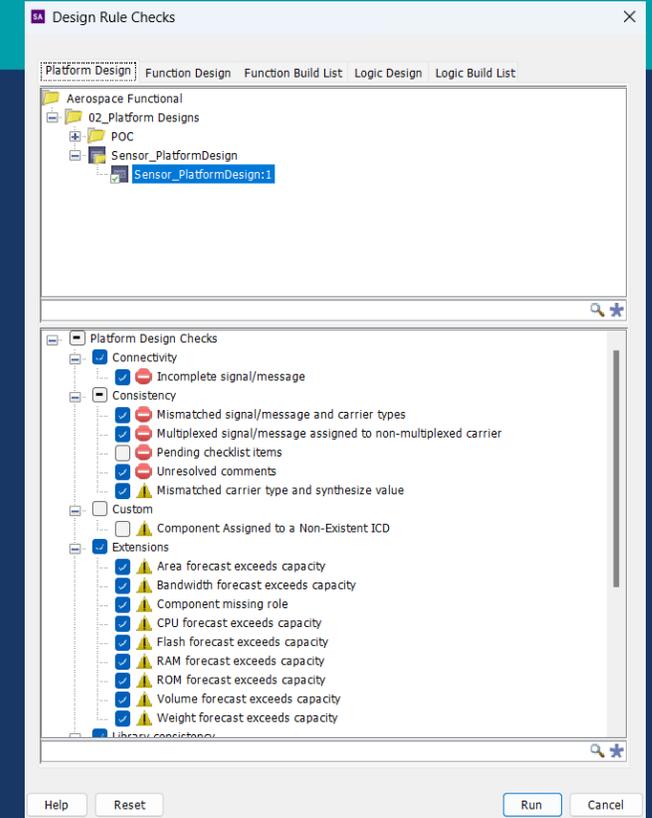
Show All Constraints [v]

Help [ ] OK [ ] Cancel [ ]

- Capture electronic topology platform capabilities (examples: device, network types)
- Automatic allocation process of captured objects by using rules
- Verify implementation feasibility using semantic checking
- Store data formally as digital twin

# Associate Functions and Signals, Validate and Optimize Architecture Capital System Architect & Capital Insights

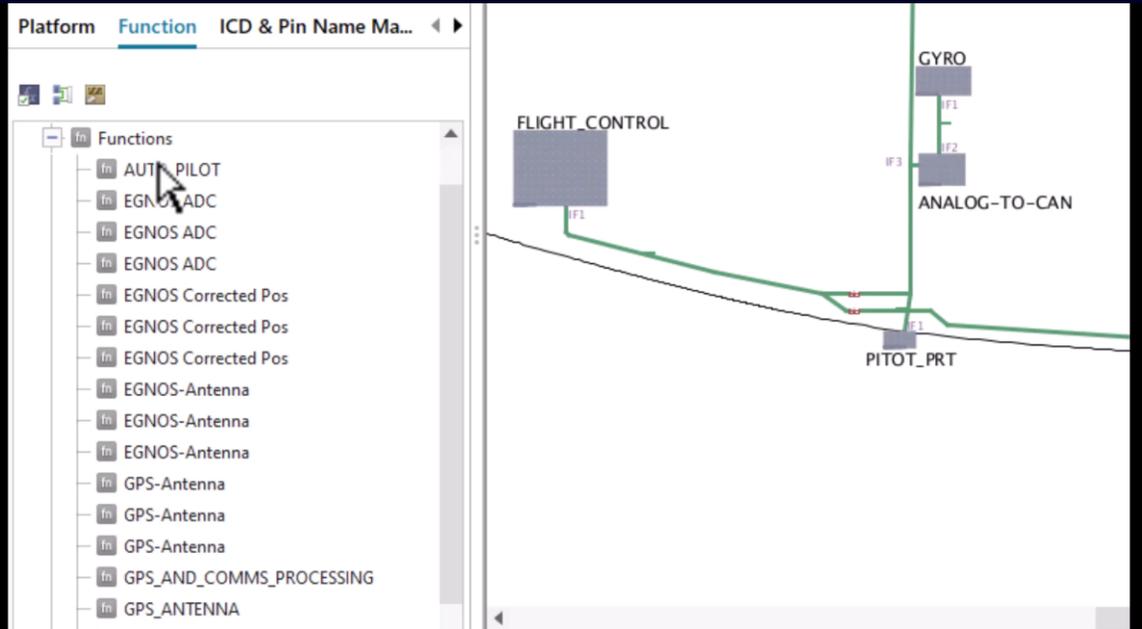
Severity	Message	Category	Check	Design/BuildList	Object
All	All	All	All	All	All
🚫	Signal <b>EgnosRaw</b> is incomplete because the topology has isolated sections. Partial route: <b>Group1, Group2</b>	Connectivity	Incomplete signal/message	Sensor_PlatformDesign:1	EgnosRaw
🚫	Signal <b>SIGNAL301</b> is incomplete because Function <b>EGNOS_PROCESSING</b> is not allocated	Connectivity	Incomplete signal/message	Sensor_PlatformDesign:1	SIGNAL301
🚫	Message <b>MESSAGE400</b> is incomplete because Function <b>EGNOS_PROCESSING</b> is not allocated	Connectivity	Incomplete signal/message	Sensor_PlatformDesign:1	MESSAGE400
⚠️	Role not defined for <b>ANALOG-TO-CAN</b>	Extensions	Component missing role	Sensor_PlatformDesign:1	ANALOG-TO-CAN
⚠️	Role not defined for <b>PITOT_PRT</b>	Extensions	Component missing role	Sensor_PlatformDesign:1	PITOT_PRT
⚠️	Role not defined for <b>PITOT_SBD</b>	Extensions	Component missing role	Sensor_PlatformDesign:1	PITOT_SBD
⚠️	Role not defined for <b>FLIGHT_CONTROL</b>	Extensions	Component missing role	Sensor_PlatformDesign:1	FLIGHT_CONTROL
⚠️	Role not defined for <b>RF_ANTENNA</b>	Extensions	Component missing role	Sensor_PlatformDesign:1	RF_ANTENNA



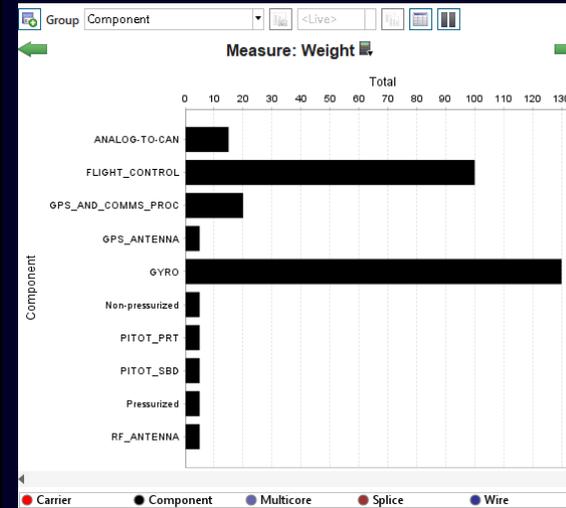
- Reducing errors that pass to next phases of product engineering, the earlier an error is detected, the easiest to solve it.
- Create custom DRC to adapt to project needs

# Associate Functions and Signals, Validate and Optimize Architecture

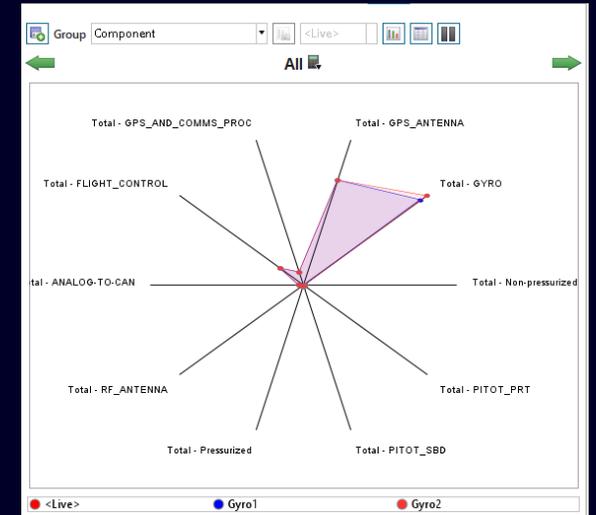
## Capital System Architect & Capital Insights



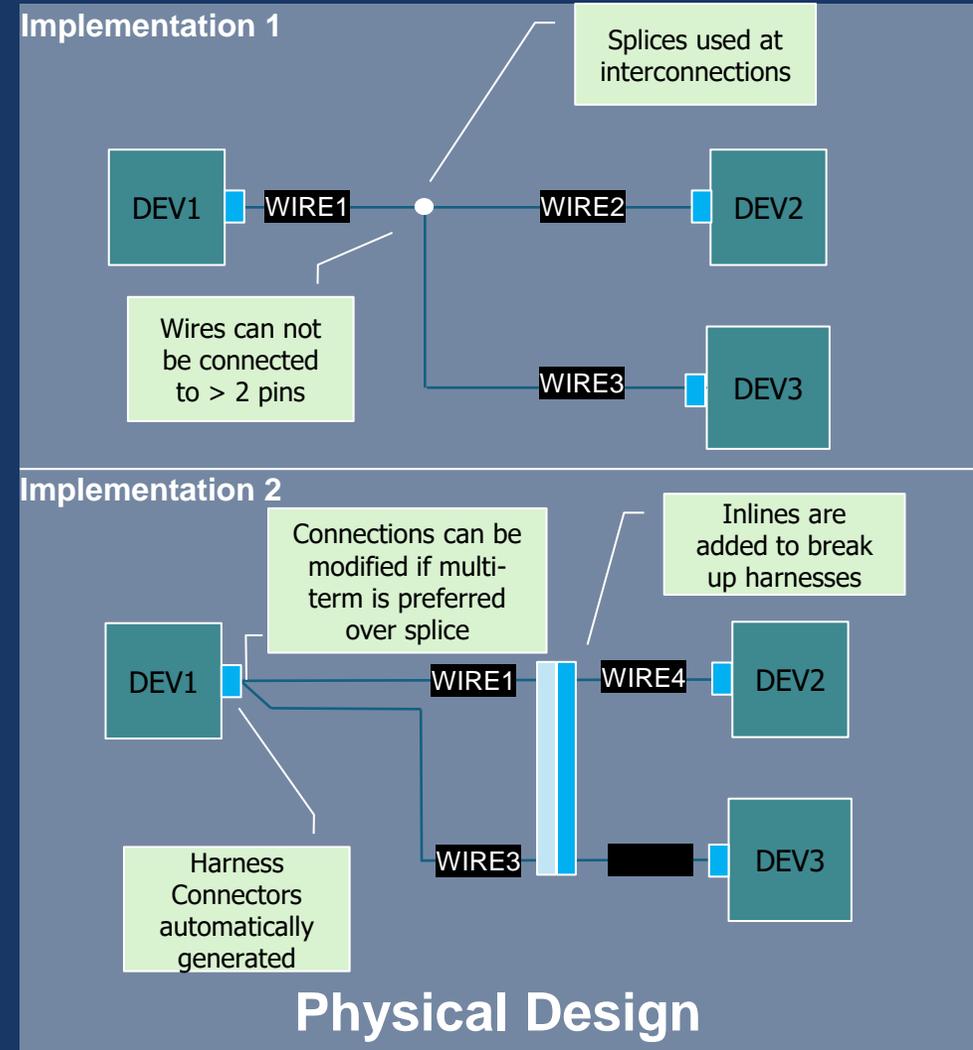
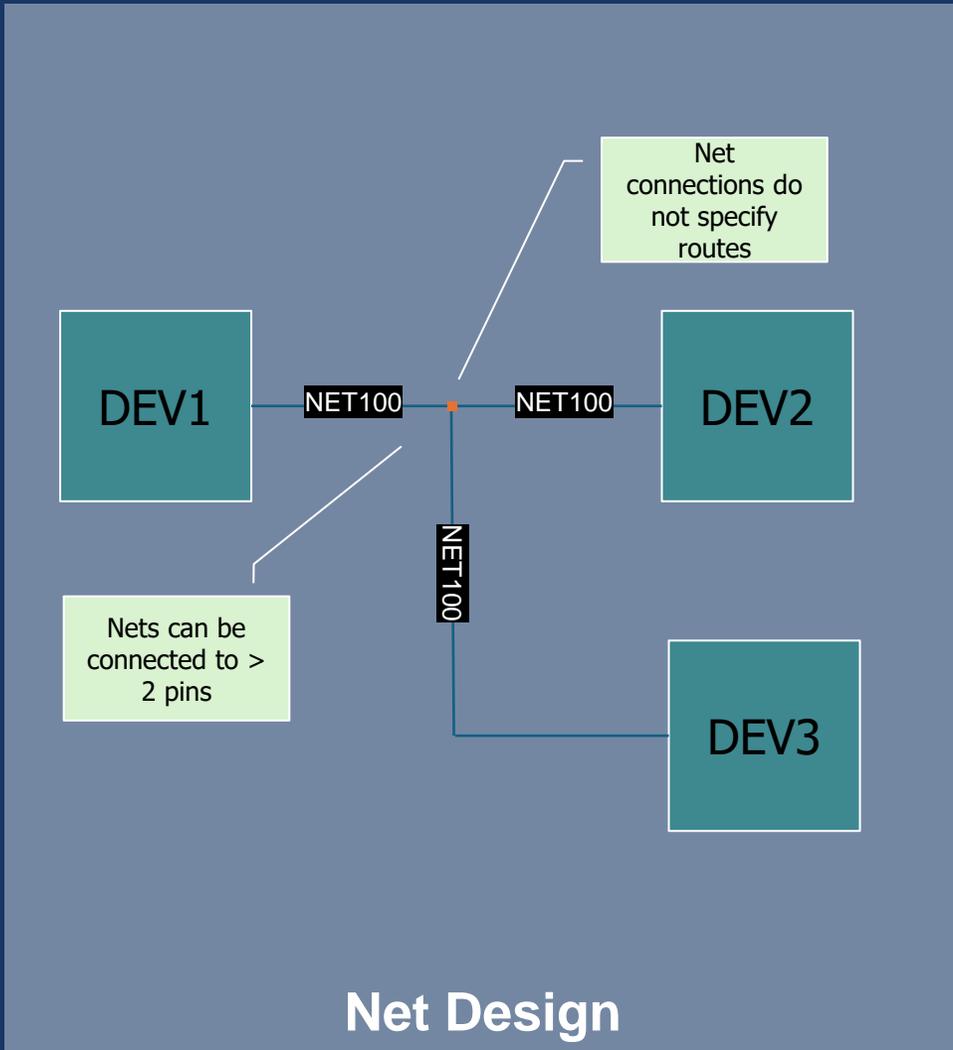
- Key metrics display



- Compare different scenarios



- Associate Functions and Signals by “Drag and Drop” or automate it with predefined rules
- Study different scenario metrics with Capital Insights
- Optimize the system based on Capital Insights results



# Integrated E/E System Development Process

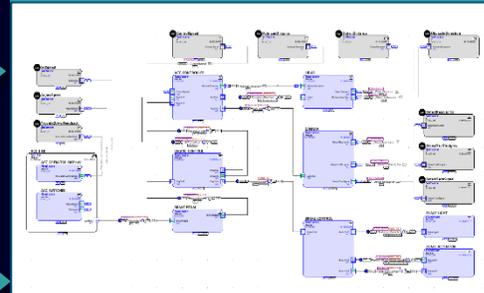
### Requirement Management & System Modelling



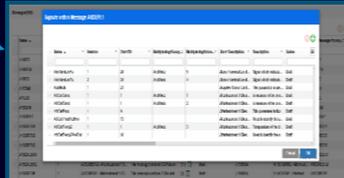
Capture & enrich functional models with their requirements

### Enrich Functional System Models

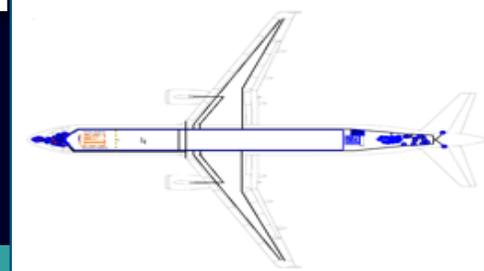
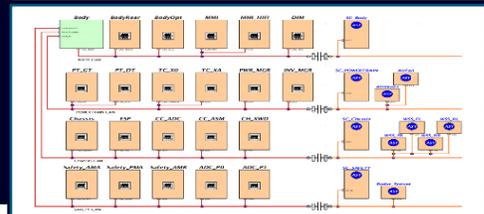
- Enrichments**
- Network Signals
  - Electrical Signals
  - IO Hardware
  - Power Distribution



### Dictionary

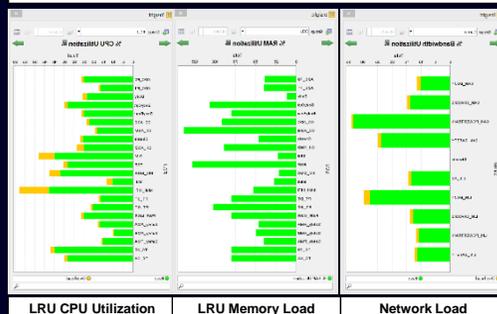


### Develop EE Architecture



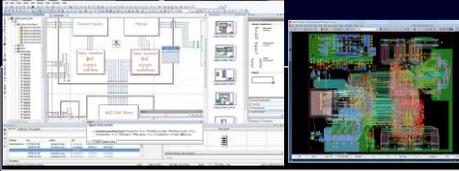
- Synthesize Logical Architectures
- Within Physical Context (↔ MCAD)
- Define Network & Ground Carriers

### Domain Metrics



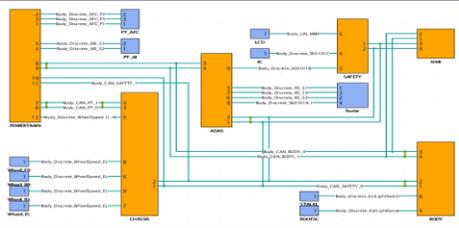
Physical Metric Forecast (Space, Cost, Weight, Length)  
 Software Metric Forecast (RAM/ROM/FLS, Performance)  
 Network Metric Forecast (Load), Design Rule Checks

### Multi-Board System Design



### Networks & SW Architecture

Component	Network	SW	Architecture
...	...	...	...
...	...	...	...



### Electrical - System Logic

Physical Implementation

- 7 PCB Design
- 7 Capital Network AUTOSAR & Network Design
- 7 Capital Design Electrical Implementation

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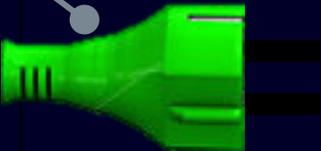
Closure and Q&A

# Importing Data From 3rd Party Modeling Tools

## Plug & Socket Importing Data From Modeling Tools

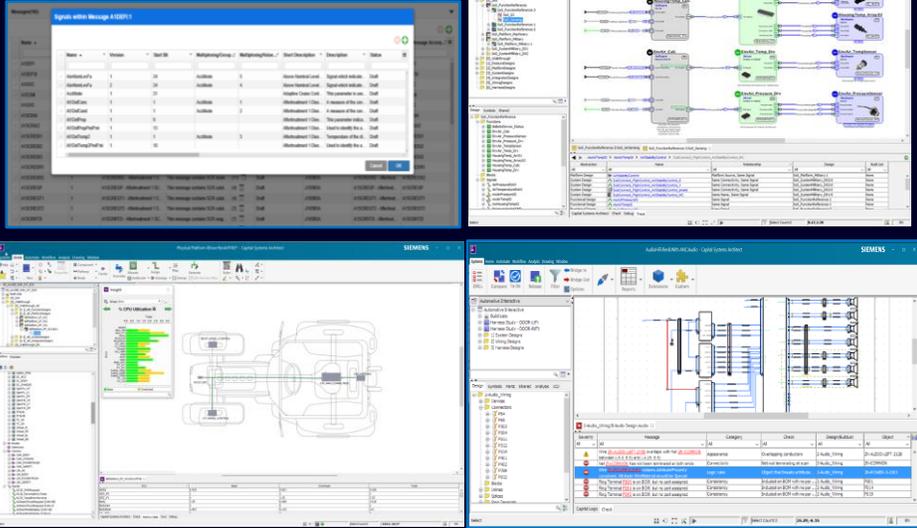
Example Input  
XMI (XML)

X2ML into Capital



### Formats

- ✓ UML
- ✓ SysML
- ✓ ARXML
- ✓ Excel
- ✓ DBC
- ✓ On demand

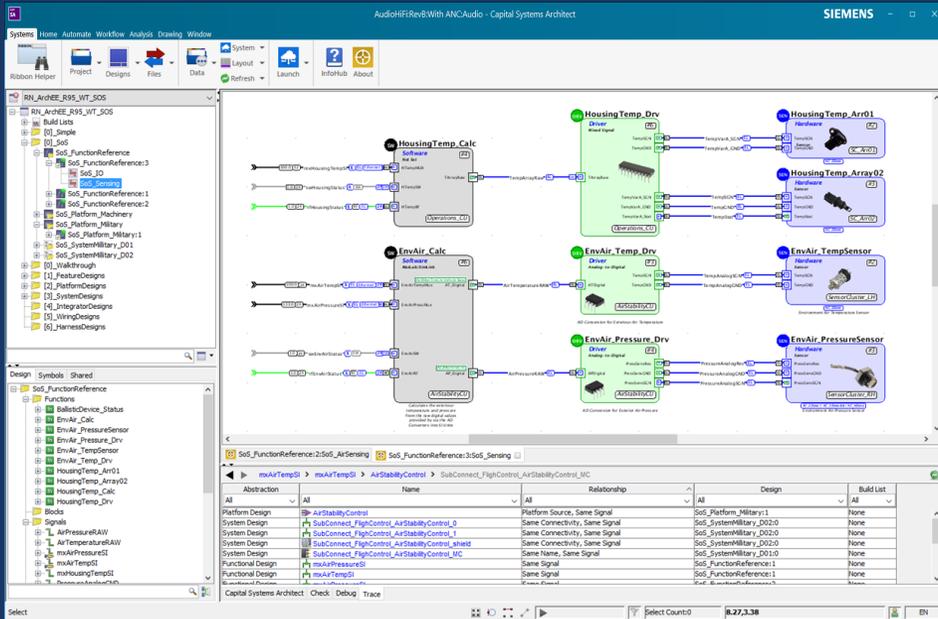


# Live Demo

Topic

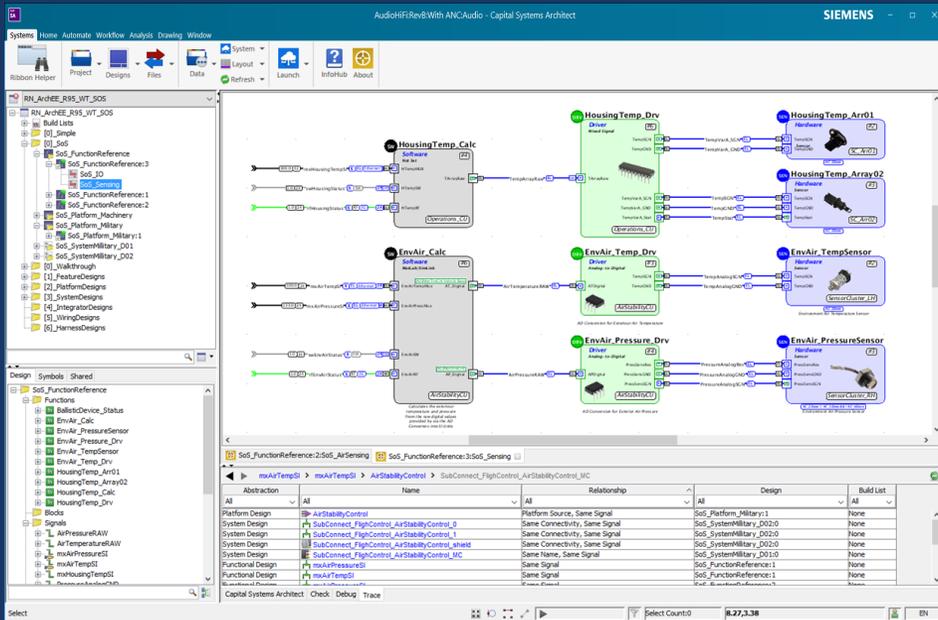
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Closure and Q&A



- Breaking into System of Systems
- Define individual blocks for each function

# Live Demo

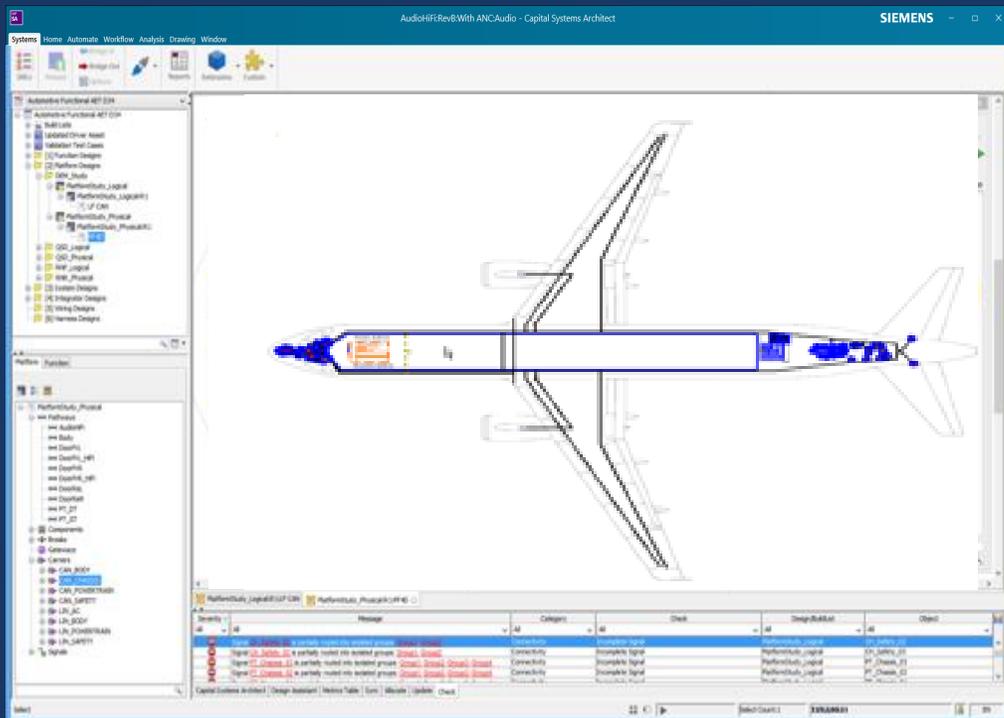


- Obtain electrical systems from systems design
- Simplify the design by dividing into individual systems
- Import, create and manage functional designs

Topic

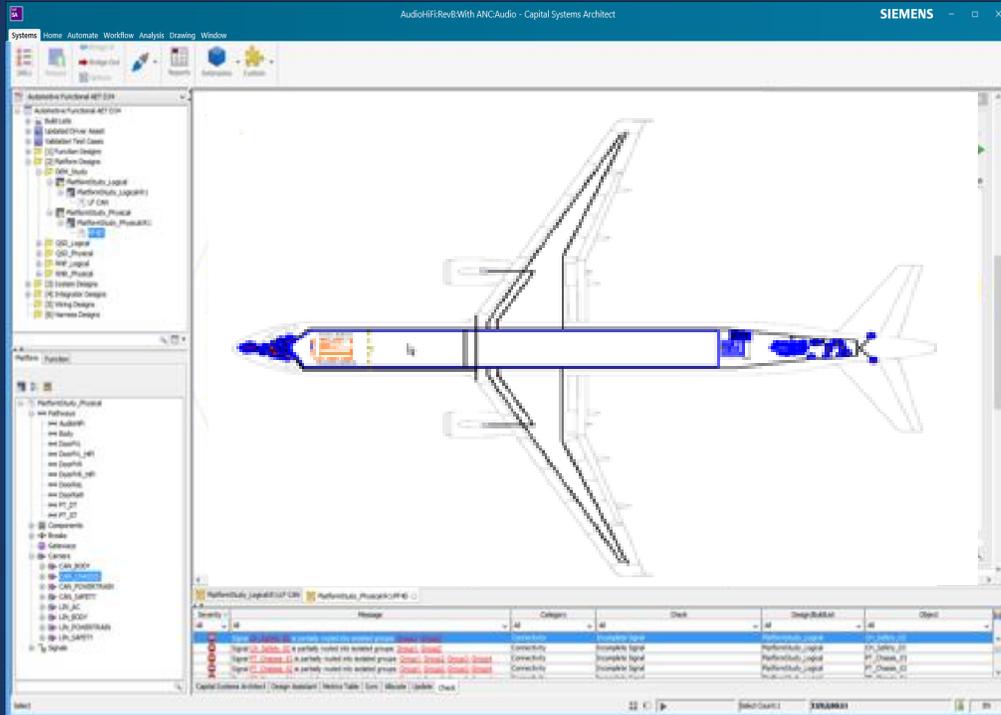
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Closure and Q&A



- Place functions and signals into components
- Analyse platform design
- Generate logical diagram

# Live Demo



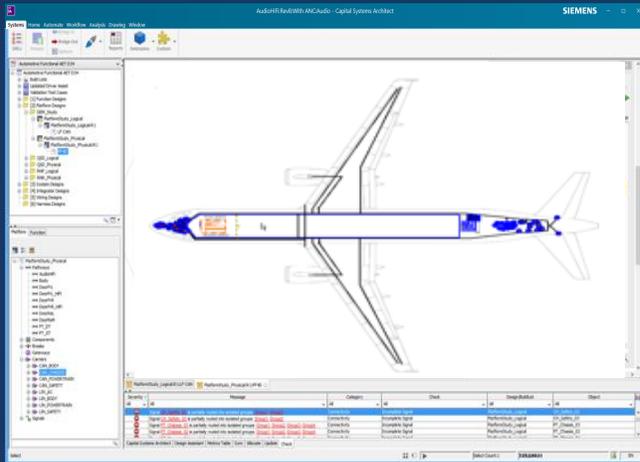
- Deploy functions and signals in components and nets
- Optimise the platform design
- Provides implementations proposals

Topic

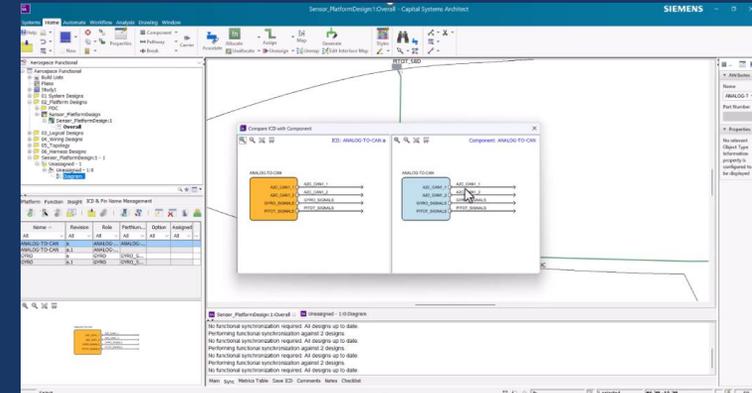
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Closure and Q&A

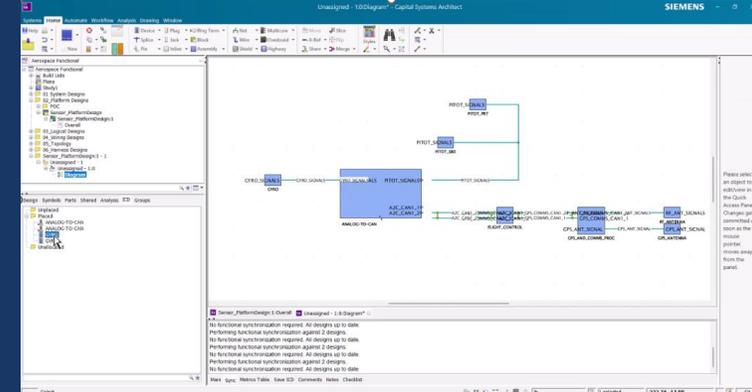
Capital System Architecture

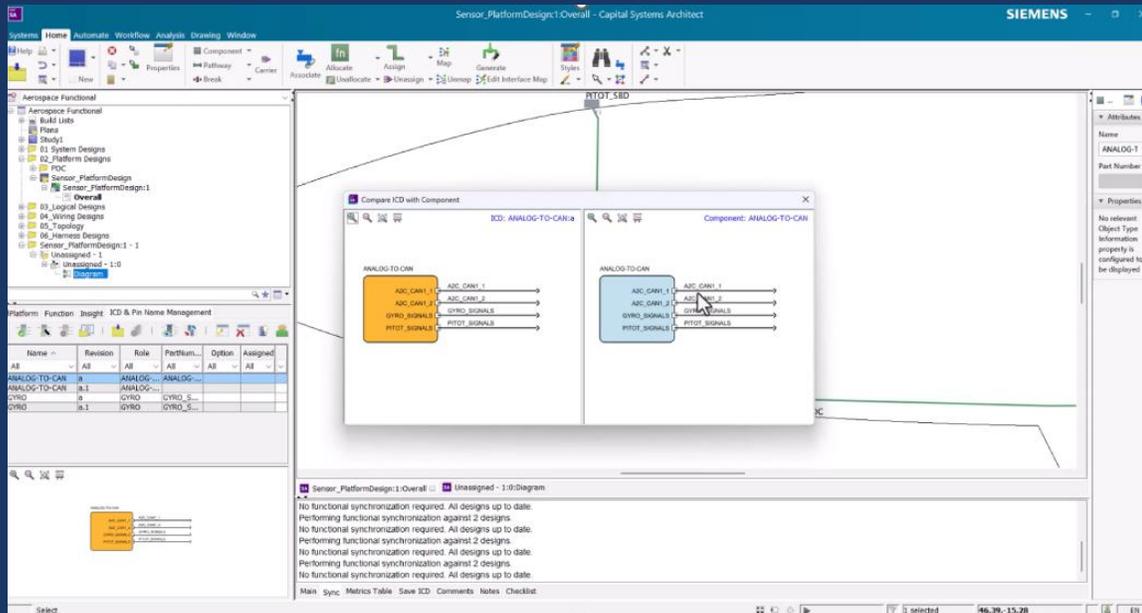


ICD

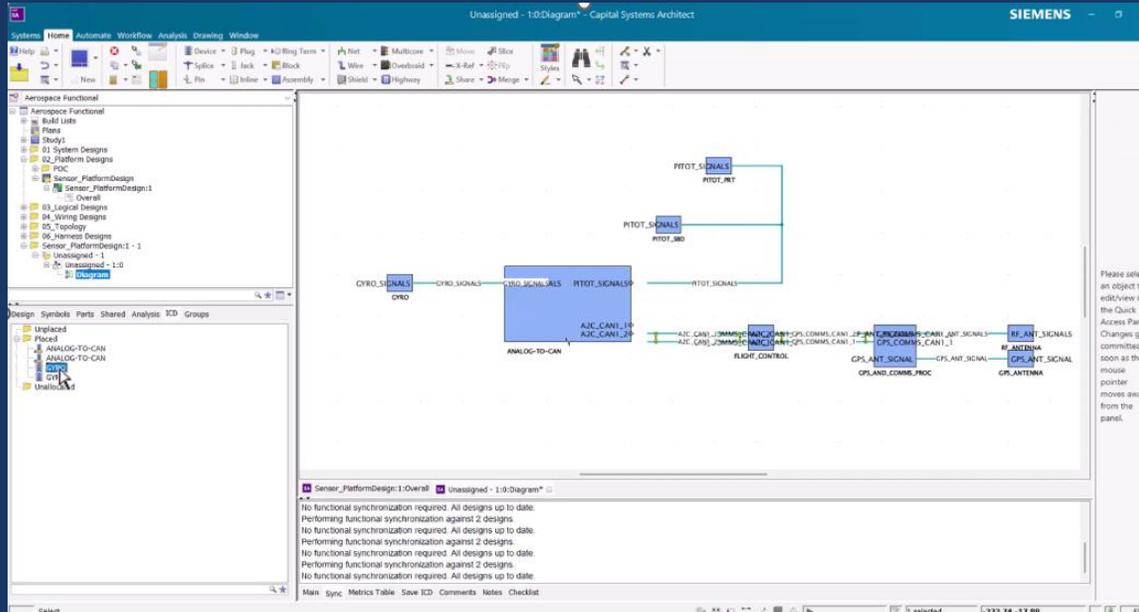


Logic Generation





- ICD creation from System Architecture
- Update logic from ICD
- Generate logical diagram



- **Generate logical diagram automatically**
- **Keep Carrier data from CSA**

# Live Demo

# Pin Mapping and ICD Creation

MAY 28<sup>th</sup>

- Display all the ICDs assigned to the project
- Assign CSA components to the ICD

The screenshot shows the 'Assign Selected ICD to Selected Component' dialog box with a table of assignments. Below the dialog, a schematic diagram shows a component labeled 'FLIGHT CONTROL' connected to an ICD.

Platform	Function	ICD & Pin Name Management	Insight
All	All	All	All
ANALO...	a.1	ANALO...	
ANALO...	a	ANALO...	
GYRO	a	GYRO	
GYRO	a.1	GYRO	

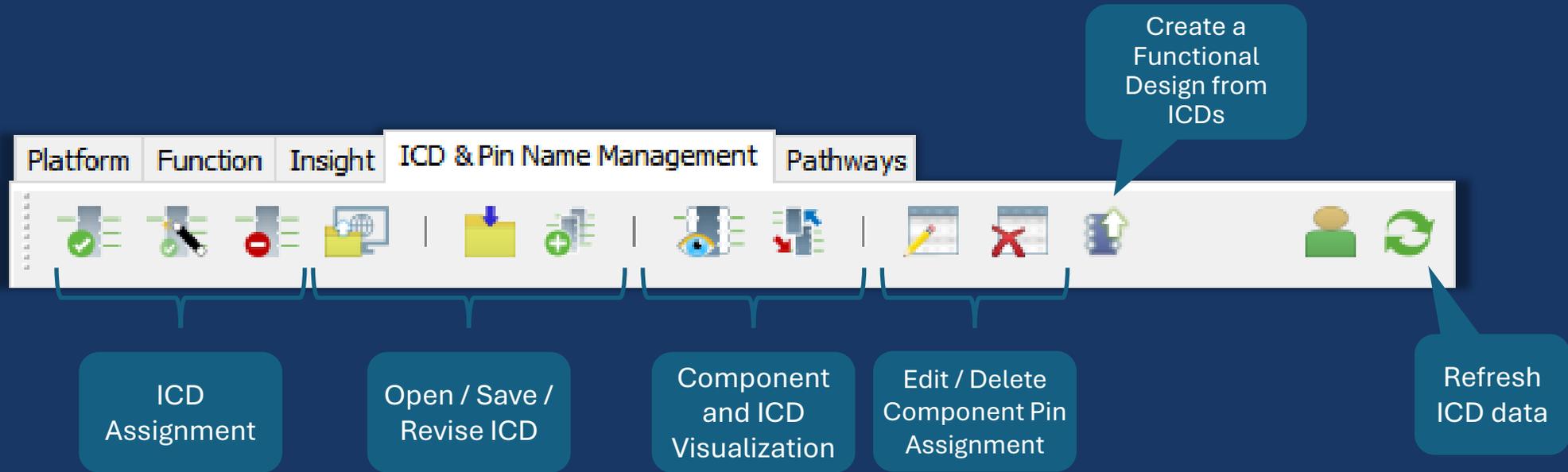
The screenshot shows the 'Compare ICD with Component' dialog box. The left pane shows the ICD 'ANALOG-TO-CAN:a' with pins A2C\_CAN1\_1, A2C\_CAN1\_2, GYRO\_SIGNALS, and PITOT\_SIGNALS. The right pane shows the component 'GPS\_ANTENNA' with a pin named GPS\_ANT\_SIGNAL. A red arrow indicates the mapping from the ICD pin to the component pin.

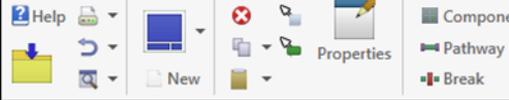
- Compare ICD with CSA Component

The screenshot shows the 'Electrical Pin Details (ANALOG-TO-CAN)' dialog box with a table of pin details.

Electrical Pin Name	Net	Carrier/Signal	Cable P/N	Wire Color
GYRO_SIGNALS	GYRO_SIGNALS	GYRO_SIGNALS		
PITOT_SIGNALS	PITOT_SIGNALS	PITOT_SIGNALS		
A2C_CAN1_1	A2C_CAN1_1	A2C_CAN1	CR-MC-CANHI	(code=R)
A2C_CAN1_2	A2C_CAN1_2	A2C_CAN1	CR-MC-CANHI	B_Black

- Modify CSA pin name to Device pin name





AutoMap will map pins based on matching Component Carrier/Signal name and ICD Net/Wire name

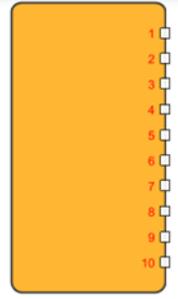
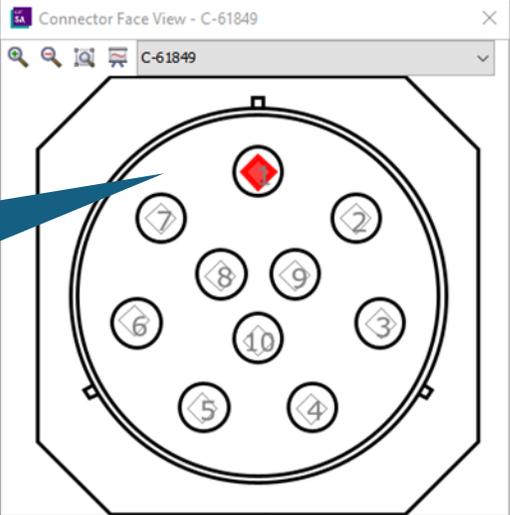


Electrical Pin Name	Net	Carrier/Signal	Cable P/N	Wire Color
<input checked="" type="checkbox"/> CR_Power	CR_Power	<input checked="" type="checkbox"/> CR_Power		
<input checked="" type="checkbox"/> CR_Data_1	CR_Data_1	<input checked="" type="checkbox"/> CR_Data		Blue-White
<input checked="" type="checkbox"/> CR_Data_2	CR_Data_2	<input checked="" type="checkbox"/> DATA-BUS		
<input checked="" type="checkbox"/> CR_Data_3	CR_Data_3	<input checked="" type="checkbox"/> CR_Data		BLUE
<input checked="" type="checkbox"/> CR_Data_4	CR_Data_4	<input checked="" type="checkbox"/> Data		Orange-White
<input checked="" type="checkbox"/> CR_Data_5	CR_Data_5	<input checked="" type="checkbox"/> Data		ORANGE
<input checked="" type="checkbox"/> CR_Data_6	CR_Data_6	<input checked="" type="checkbox"/> Data		Green
<input checked="" type="checkbox"/> CR_Data_7	CR_Data_7	<input checked="" type="checkbox"/> Data		Green-White
<input checked="" type="checkbox"/> CR_Data_8	CR_Data_8	<input checked="" type="checkbox"/> Data		Brown-White
<input checked="" type="checkbox"/> CR_Data_9	CR_Data_9	<input checked="" type="checkbox"/> Data		Brown1
<input checked="" type="checkbox"/> CR_Data_10	CR_Data_10	<input checked="" type="checkbox"/> Data		

Select desired Component Electrical Pin Name

Pin Name	Mated C...	Nets/Wires	PinName
<input checked="" type="checkbox"/> 1	C-61849:1		1
<input checked="" type="checkbox"/> 2	C-61849:2		2
<input checked="" type="checkbox"/> 3	C-61849:3		3
<input checked="" type="checkbox"/> 4	C-61849:4		
<input checked="" type="checkbox"/> 5	C-61849:5		
<input checked="" type="checkbox"/> 6	C-61849:6		
<input checked="" type="checkbox"/> 7	C-61849:7		
<input checked="" type="checkbox"/> 8	C-61849:8		
<input checked="" type="checkbox"/> 9	C-61849:9		
<input checked="" type="checkbox"/> 10	C-61849:10		10

Select desired ICD Pin



ArchitectureDesign1::Diagram1\*  
Performing functional synchronization against design FunctionDesign1:-.  
No functional synchronization required. All designs up to date.

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Closure and Q&A

# Integrated E/E System Development Process

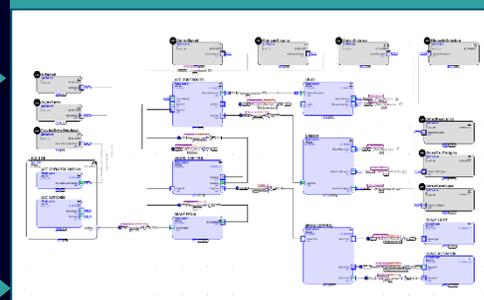
### Requirement Management & System Modelling



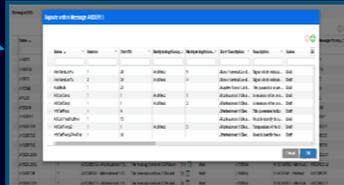
Capture & enrich functional models with their requirements

### Enrich Functional System Models

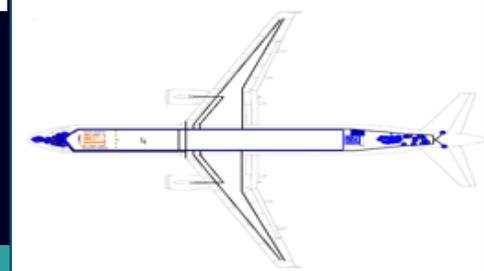
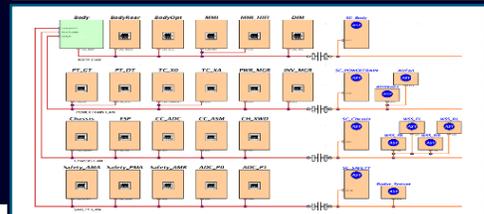
- Enrichments**
- Network Signals
  - Electrical Signals
  - IO Hardware
  - Power Distribution



### Dictionary

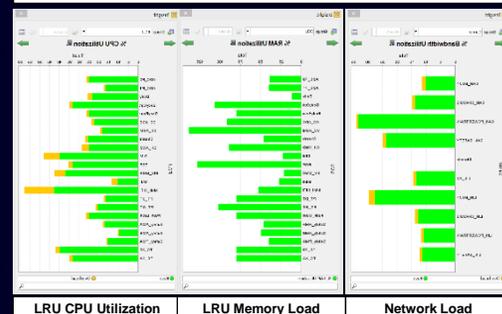


### Develop EE Architecture



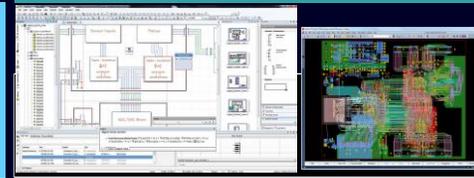
- Synthesize Logical Architectures
- Within Physical Context (↔ MCAD)
- Define Network & Ground Carriers

### Domain Metrics



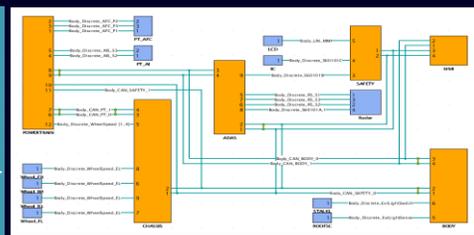
Physical Metric Forecast (Space, Cost, Weight, Length)  
 Software Metric Forecast (RAM/ROM/FLS, Performance)  
 Network Metric Forecast (Load), Design Rule Checks

### Multi-Board System Design



### Networks & SW Architecture

Component	Network	SW	Architecture
...	...	...	...
...	...	...	...
...	...	...	...



### Electrical - System Logic

Physical Implementation

- 7 PCB Design
- 7 Capital Network AUTOSAR & Network Design
- 7 Capital Design Electrical Implementation



## Capital Value Provided

Software as a Service enables the power of Xcelerator in a more accessible, scalable and flexible form.

Complete End-to-End Solution

Minimize Human Mistakes

Automate Workflow

## Thanks for your attention