CDT TECH DAY

MAY 28th

Z-Planner for Signal Integrity

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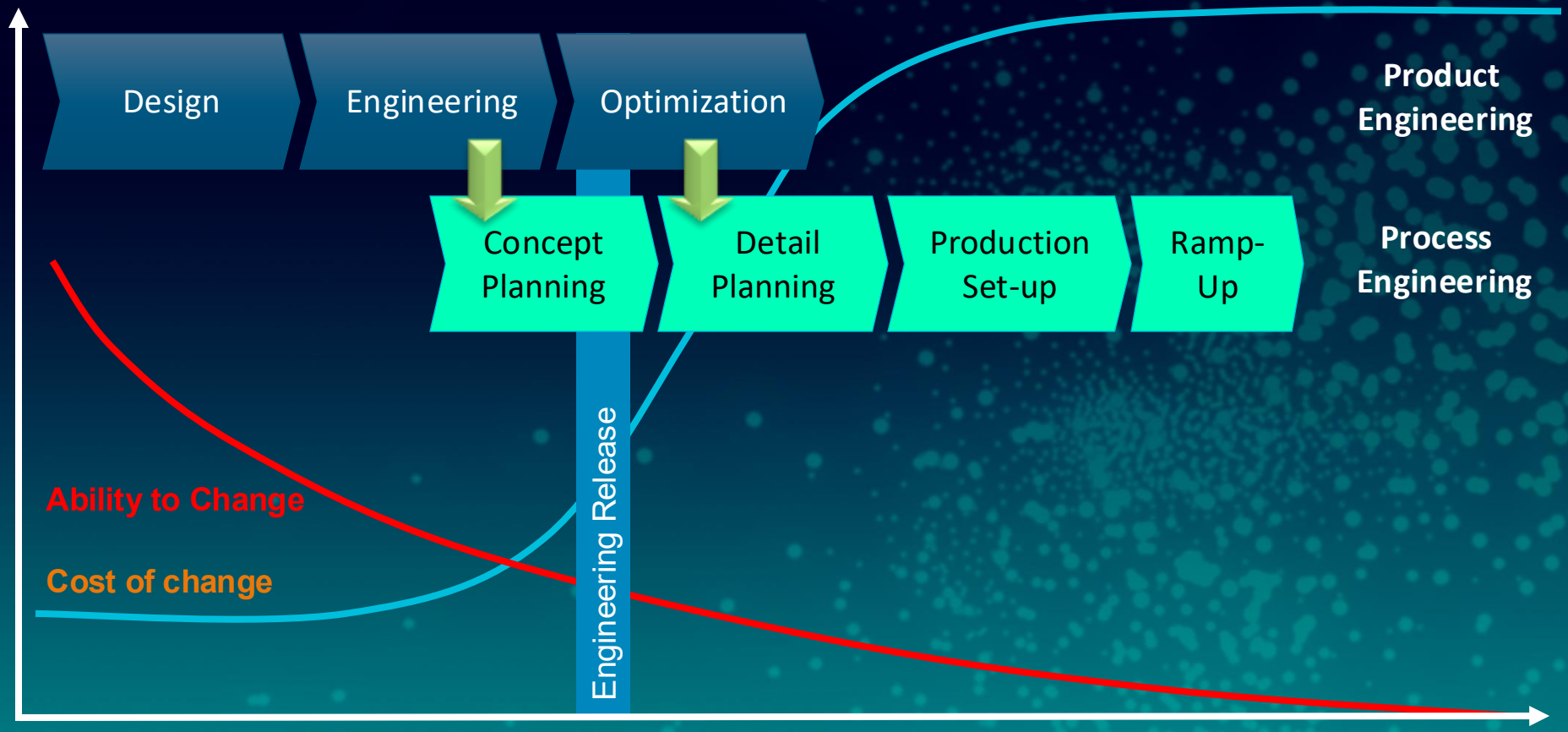
Integrate engineering and manufacturing



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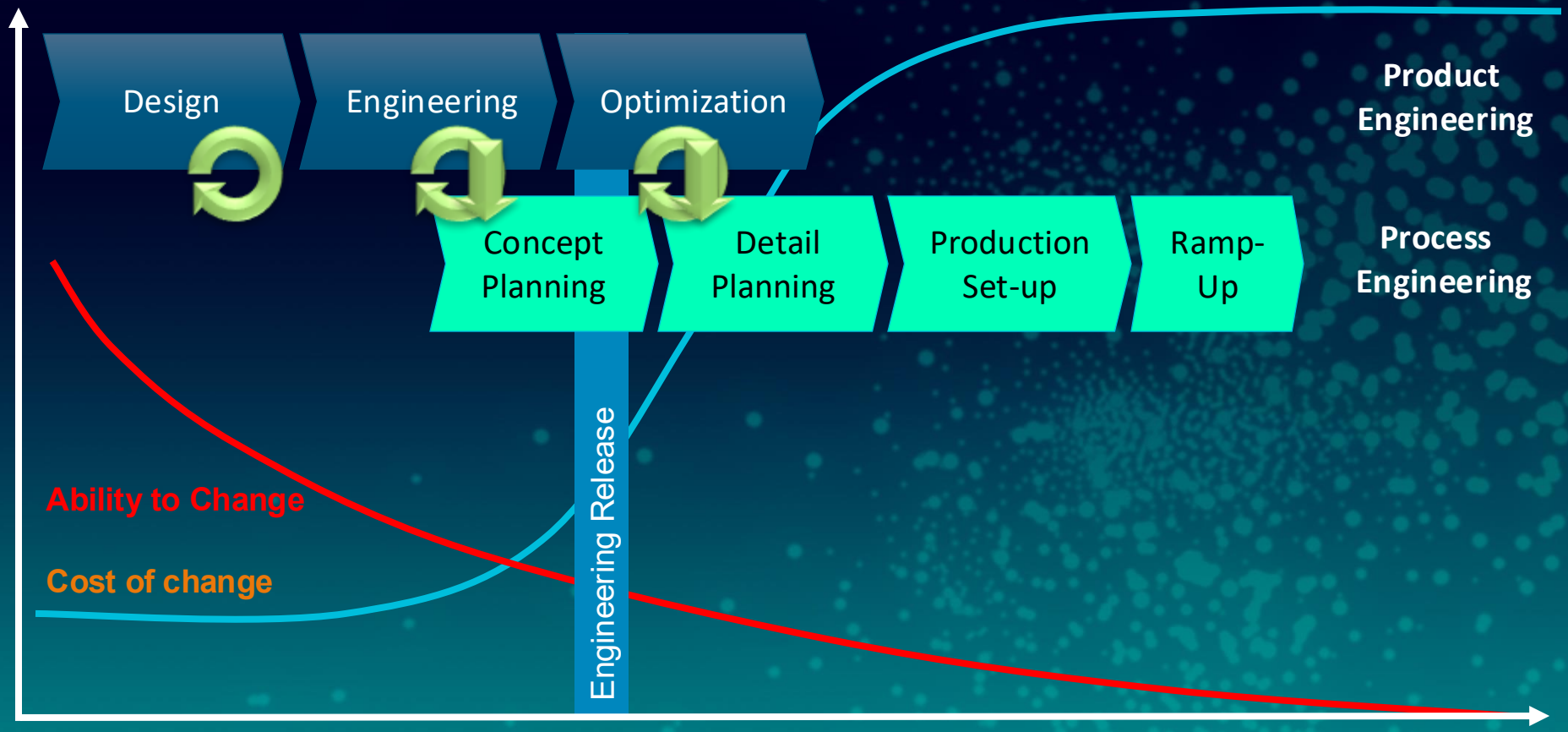
Integrate engineering and manufacturing
Shift left



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For the Entire Product Lifecycle

Valor NPI	Valor Process Preparation	APS Scheduling	Opcenter IPL	Opcenter Execution Electronics	Opcenter Intelligence
Z-Planner	Valor BOM Connector				

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Stackup Design for Signal Integrity

“Make it Real; Make it Better”

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The Stackup is Fundamental to SI Simulations

Often, the stackup used for SI simulations is not the same as the stackup the PCB fabricator will propose:

- Changes may be made to layer heights and trace widths
- Materials used will have specific values for Dk and Df that are part of a real (and purchasable) stackup
- Copper roughness will be associated with specific cores and foils
  - Prepreg on outer high-speed layers often has greater roughness on the foils than cores

If your simulations were not based on electrical characteristics of actual available materials, then their accuracy is questionable

If you have an SI failure that requires stackup changes, how do you make that recommendation based on what materials are available and what your company can buy?

- How do you add value to the material selection process?

	A	B	C	D	E	F	G	H	I	J	K
	Layer #	Type	Layer Name	Material Name	Construction	Resin (%)	Dk (f)	Df (f)	Copper Weight (oz)	Comments	Copper Foil
1		Solder Mask	SOLDERMASK_...	PFR-800 AUS402	N/A		3.90	0.0270		AIR	
2		Plating		Plating							
3	1S	Signal	SIGNAL_1	Metal			3.90	0.0000		Signal	VLP
4		Prepreg	DIELECTRIC_3	370HR	2116	56.0%	4.08	0.0200		Core/Pre-Preg	
5	2P	Plane	PLANE_2	Metal			3.26	0.0300		Plane	RTF (Primary Cu)
6		Core	DIELECTRIC_5	370HR	2116	47.0%	4.26	0.0180		Core/Pre-Preg	
7	3S	Signal	SIGNAL_3	Metal			3.26	0.0300		Signal	RTF (Primary Cu)
8		Prepreg	DIELECTRIC_7	370HR	2116	56.0%	4.08	0.0200		Core/Pre-Preg	
9	4	Plane	SIGNAL_4	Metal			3.26	0.0300		Plane	RTF (Primary Cu)
10		Core	DIELECTRIC_9	370HR	2116	47.0%	4.26	0.0180		Core/Pre-preg	
11	5S	Signal	SIGNAL_5	Metal			3.26	0.0300		Signal	RTF (Primary Cu)
12		Prepreg	DIELECTRIC_11	370HR	2116	56.0%	4.08	0.0200		Core/Pre-Preg	
13	6P	Plane	PLANE_6	Metal			3.26	0.0300		Plane	RTF (Primary Cu)
14		Core	DIELECTRIC_13	370HR	2x2116	47.0%	4.26	0.0180		Core/Pre-Preg	
15	7P	Plane	PLANE_7	Metal			3.26	0.0300		Plane	RTF (Primary Cu)
16		Prepreg	DIELECTRIC_15	370HR	2116	56.0%	4.08	0.0200		Core/Pre-Preg	
17	8S	Signal	SIGNAL_8	Metal			3.26	0.0300		Signal	RTF (Primary Cu)
18		Core	DIELECTRIC_17	370HR	2116	47.0%	4.26	0.0180		Core/Pre-Preg	
19	9	Plane	SIGNAL_9	Metal			3.26	0.0300		Plane	RTF (Primary Cu)
20		Prepreg	DIELECTRIC_19	370HR	2116	56.0%	4.08	0.0200		Core/Pre-preg	
21	10S	Signal	SIGNAL_10	Metal			3.26	0.0300		Signal	RTF (Primary Cu)
22		Core	DIELECTRIC_21	370HR	2116	47.0%	4.26	0.0180		Core/Pre-Preg	
23	11P	Plane	PLANE_11	Metal			3.26	0.0300		Plane	RTF (Primary Cu)
24		Prepreg	DIELECTRIC_23	370HR	2116	56.0%	4.08	0.0200		Core/Pre-Preg	
25	12S	Signal	SIGNAL_12	Metal			3.90	0.0000		Signal	VLP
26		Plating		Plating							
27		Solder Mask	SOLDERMASK_...	PFR-800 AUS402	N/A		3.90	0.0270		AIR	

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Make it Real

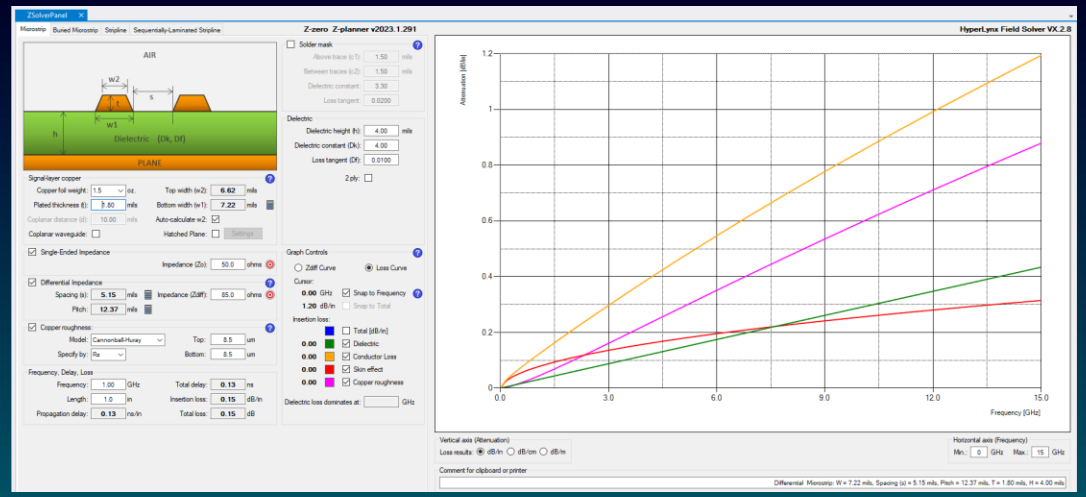
In pre-layout, how do you determine if the combination of material values you are simulating can be purchased or manufactured?

- Entering all the values from a PCB fabricator is tedious and error prone
- If changes are needed to pass SI, you have to return to the PCB fabricator for a new stackup
  - Or you might simulate something that can't be built

In post-layout, can you easily change materials within the restrictions of your company's approved suppliers?

- Have you accounted for details like surface roughness on both sides of the copper foil, prepreg layer compression, glass weave, Dk and Df at specific frequencies, etc?

Allowing these tradeoffs to be made by the SI or design engineer improves the accuracy and efficiency of the design process



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Z-planner for Stackup Design

Stackup design wizard

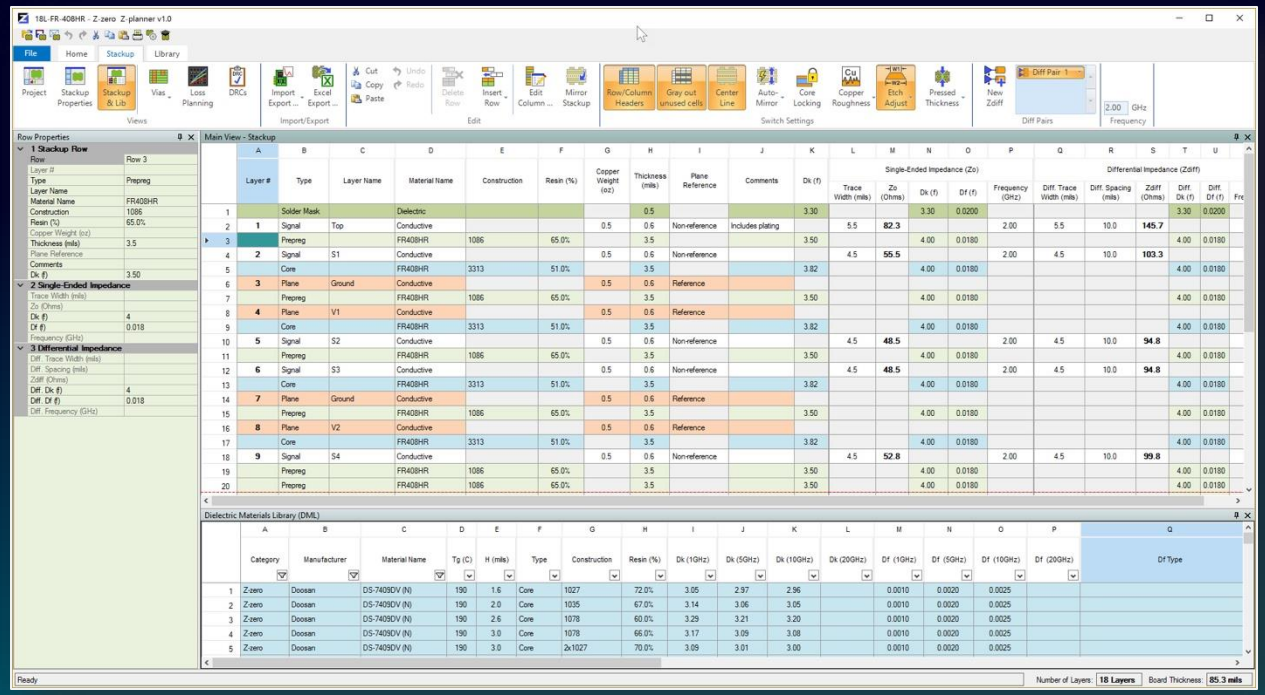
HyperLynx field solver

Complete dielectric materials library representing North American and Asian manufacturers

Dielectric material selection tool

Stackup comparison utility

DFM checks, including vias



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Z-planner Enterprise connects OEM specifications to PCB manufacturing

PLANNER Enterprise

DESIGN

MANUFACTURING

Spec

IMPEDANCE

Fab

Simulate what you're actually going to build

SIGNAL INTEGRITY REQUIREMENTS

STACKUP PROPOSAL

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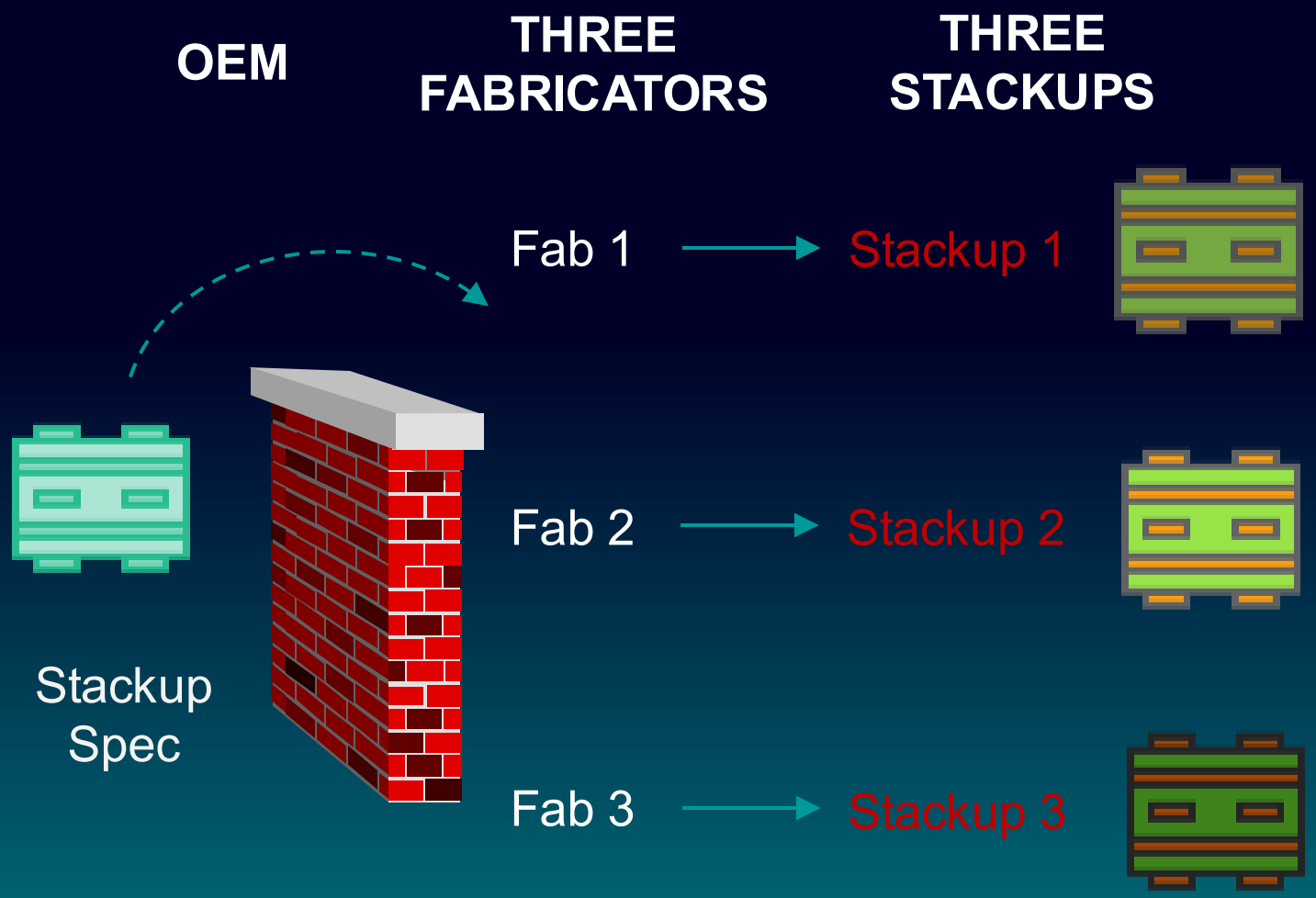

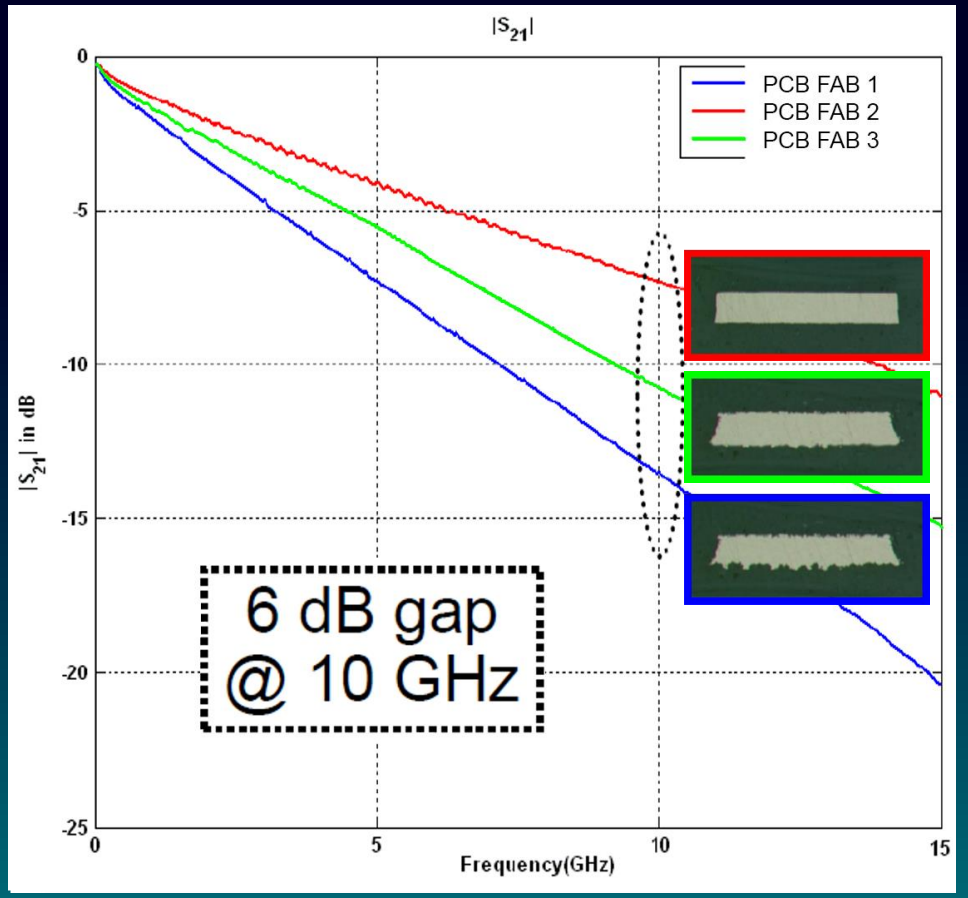

Each fabricator's stackup and materials experience drives line width and spacing proposals to achieve targeted electrical performance

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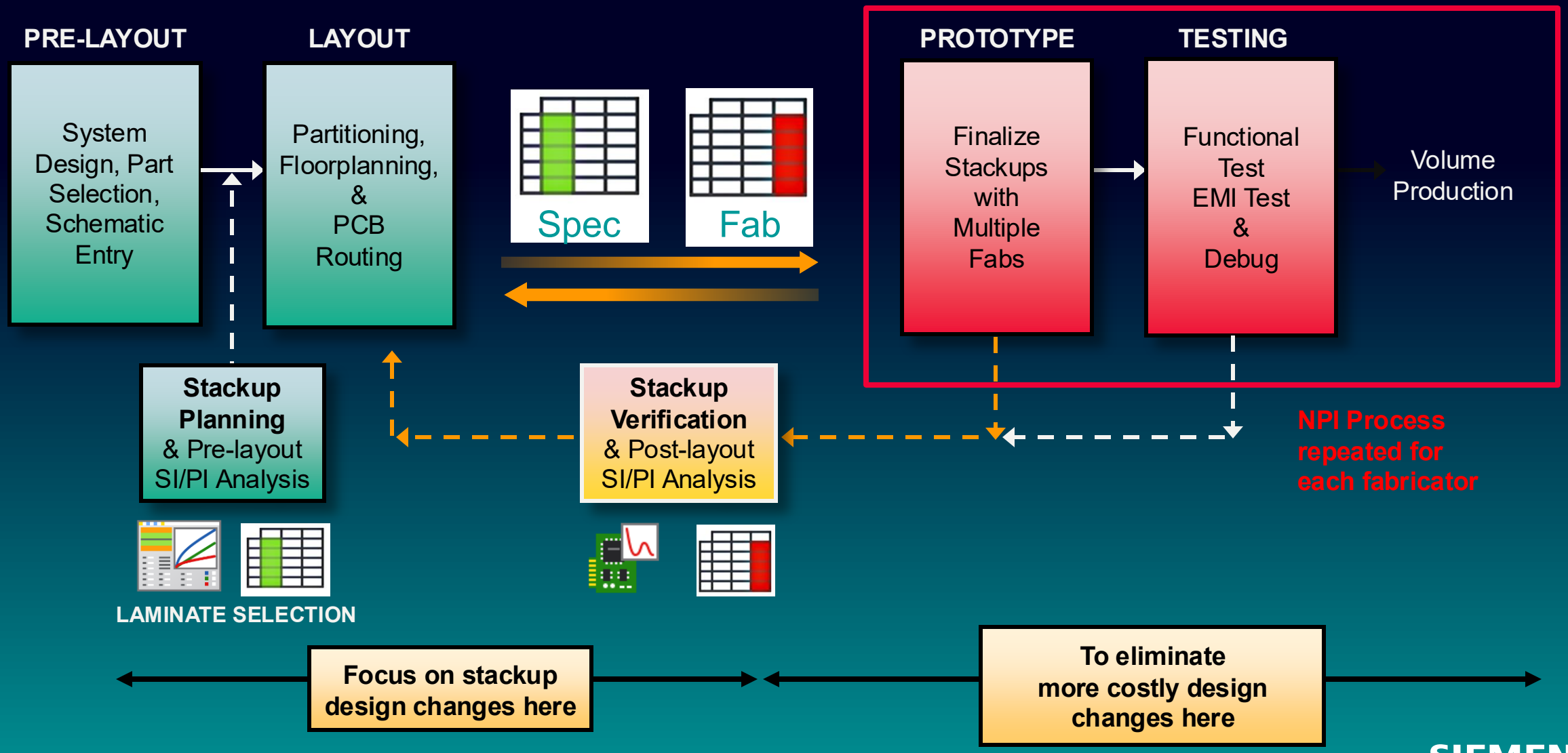
Move Stackup Design as far to the Left as Possible



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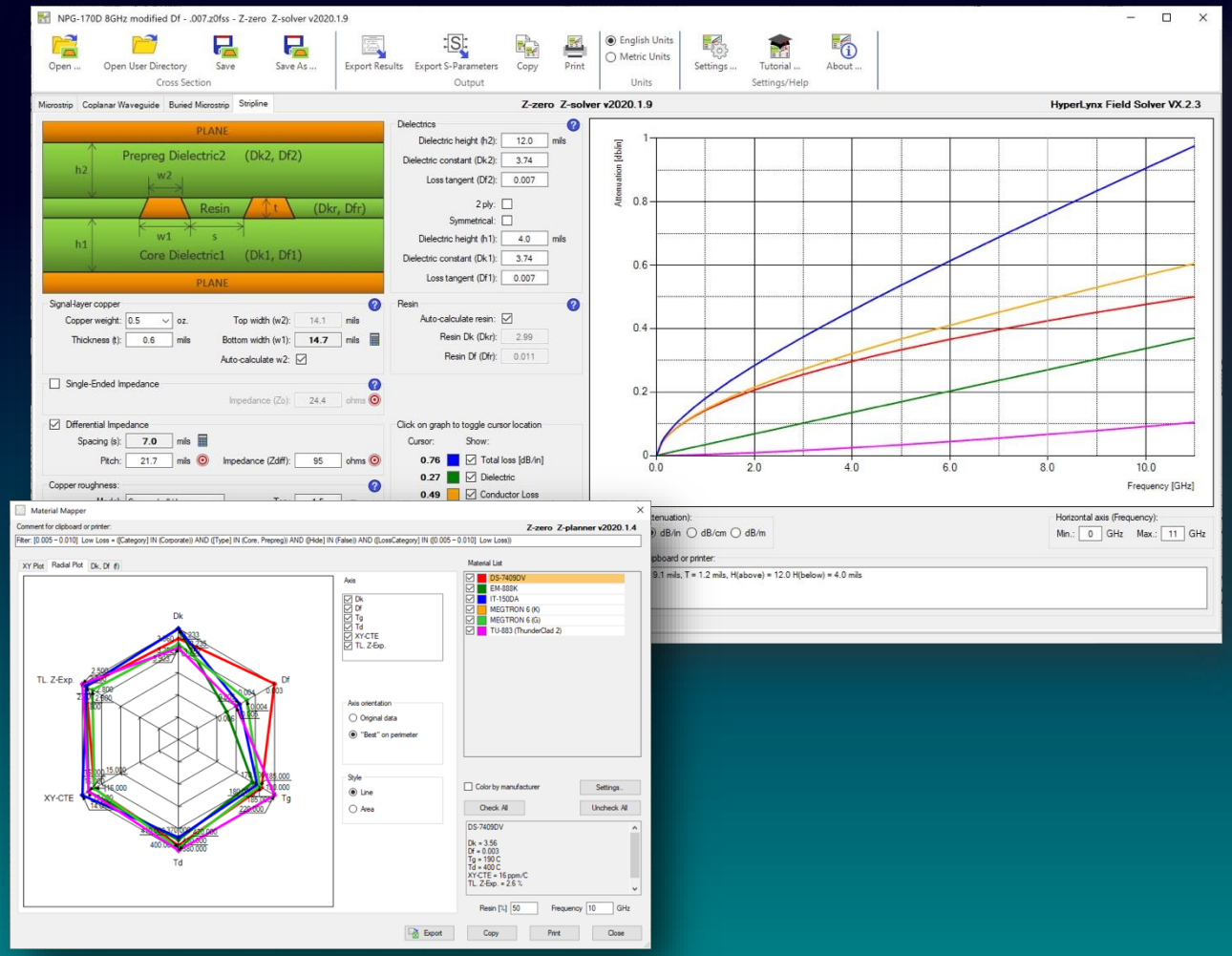
Z-planner for Stackup Design

Easy-to-use tool for pre-layout impedance and loss planning

- Optimize single-ended and differential impedances
- Dial in material requirements

HyperLynx field solver

- Latest advances in copper roughness modeling
- S-parameter export of traces for SI simulation
- Frequency, resin content, glass style, and pressed prepreg thickness taken into account



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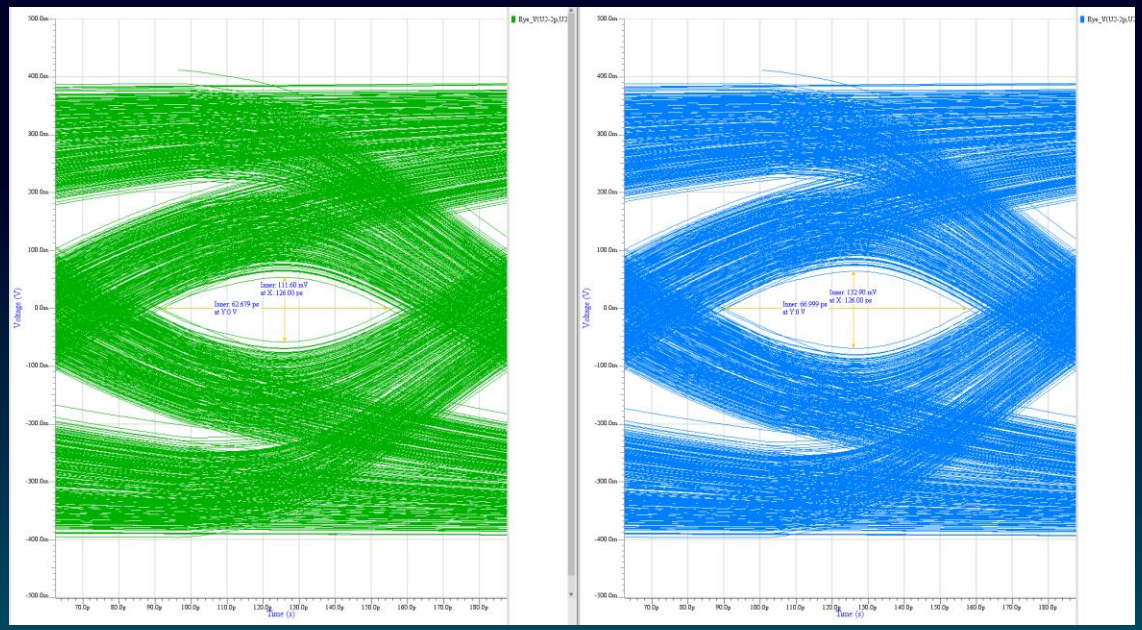
Analysis Example – Make it Real

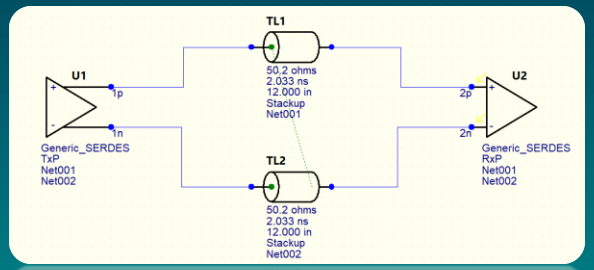
Suppose you are designing a SerDes net over 12 inches of trace at 8GBs

- Using a starting stackup with typical values gives one eye
  - Blue - Eye height = 132.5 mv, eye width = 67 ps
- Changing to similar values but with *real materials* give a somewhat different eye
  - Green - Eye height = 111.6 mv, eye width = 62.7 ps
- 18.7% worse eye height with real materials



If it was easy to use real materials, why not simulate something closer to reality?

- Extensive searching capability in Z-planner allows you to quickly find materials based on:
  - Manufacturer or material name
  - Dielectric height
  - Dk or Df
  - Surface roughness
  - Thermal characteristics
  - Etc.



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Analysis Example – Make it Better

If you want more margin in the eye diagram, what values would you change?

- Dissipation factor (Df), surface roughness?

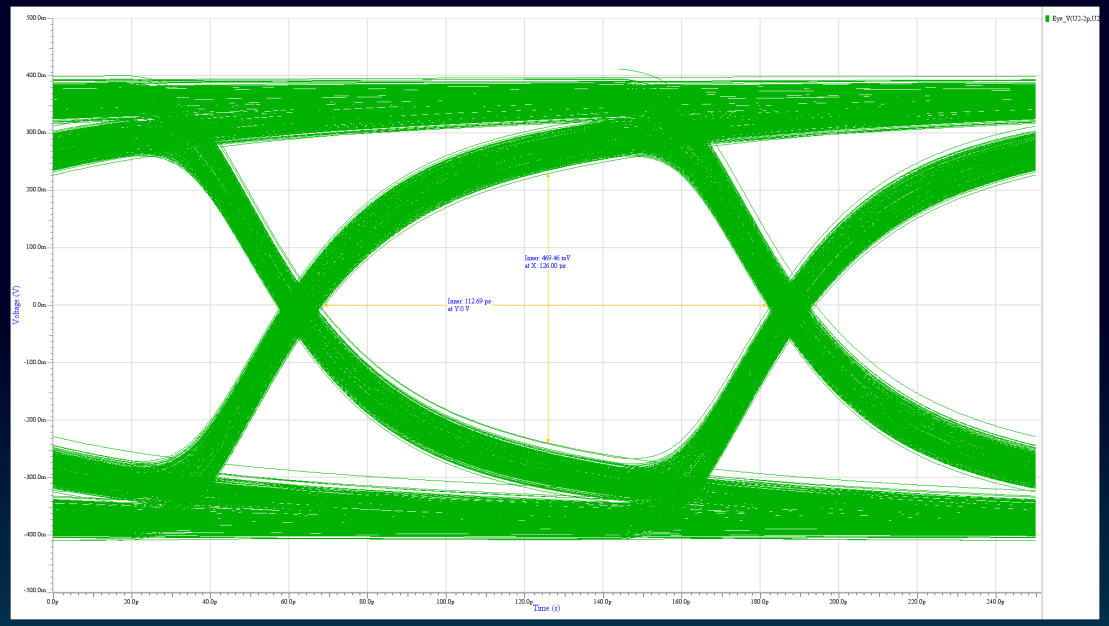
If you change Df:

- What materials have a similar height and Dk?
- How do you find a combination of improved values that you can still build?

Z-planner makes it easy to substitute higher performance materials and then simulate with real values

Eye Diagram and PCIe Compliance metric

- Green plot - Eye height = 469 mv, Eye width = 112.7 ps
- PCIe3 Compliance with equalization:
  - Old stackup - Eye height = 98.5 mV, Eye width = 0.606 UI
  - New stackup - Eye height = 168 mV, Eye width = 0.611 UI



Eye width/height measured at BER 1e-12 - Full Swing

		TX / RX Pins		Eye Height				Eye Width		
#	Channel	TX	RX	Min Required [V]	Measured [V]	Pass/Fail	Measured At Offset [UI]	Min Required [UI]	Measured [UI]	Pass/Fail
	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
1	Net001 / Net002	U1.1p U1.1n	U2.2p U2.2n	0.025	0.0985423	PASSED	-0.0138889	0.3	0.606481	PASSED

Eye width/height measured at BER 1e-12 - Full Swing

		TX / RX Pins		Eye Height				Eye Width		
#	Channel	TX	RX	Min Required [V]	Measured [V]	Pass/Fail	Measured At Offset [UI]	Min Required [UI]	Measured [UI]	Pass/Fail
	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
1	Net001 / Net002	U1.1p U1.1n	U2.2p U2.2n	0.025	0.167934	PASSED	-0.00694444	0.3	0.611111	PASSED

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Z-planner Lets You Model Your Board “As Fabricated”

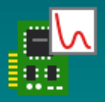
Vias, plating, and the sequential-lamination process are explicitly accounted for

- Via definitions include laser-drilled microvias and mechanically-drilled through-hole vias, blind and buried vias, as well as front/back drilled through-hole vias 
- Via DFM checks provide immediate manufacturability feedback for unconventional via constructions 

- Core and prepreg checks that align with the PCB manufacturing process
- Prepreg height adjustments according to retained (%) copper 
- Plating requirements accounted for and modeled with the HyperLynx 2D field solver 

Copper roughness for all surfaces accounted for

- Core-side roughness
- Prepreg-side roughness 

- Build-up layer roughness
- Plating roughness
- Loss modeled with the HyperLynx 2D field solver 
- Exported to HyperLynx SI for detailed time- and frequency-domain simulation 

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Summary of Z-planner for SI Engineers

PLANNER Enterprise

Extensive Capabilities

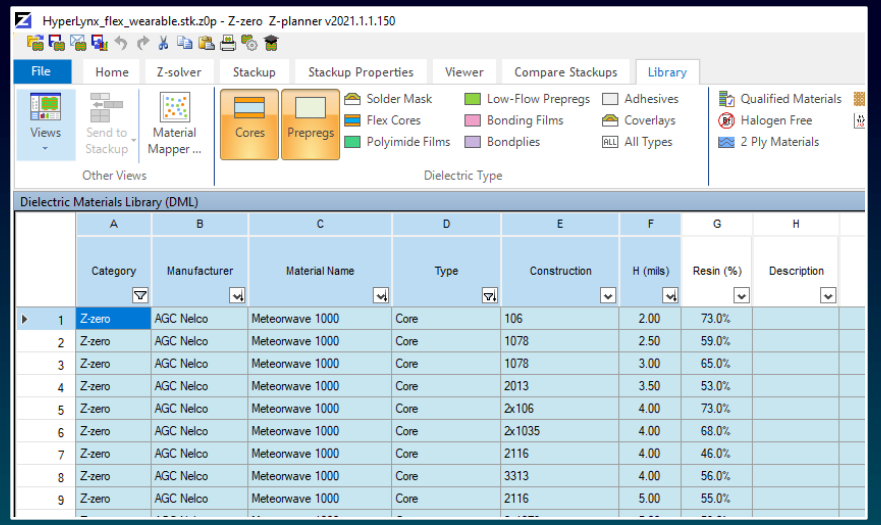
- Z-planner Enterprise addresses entire stackup and PCB design flow
- Improves communication and collaboration with fabricators

PCB Laminate Libraries

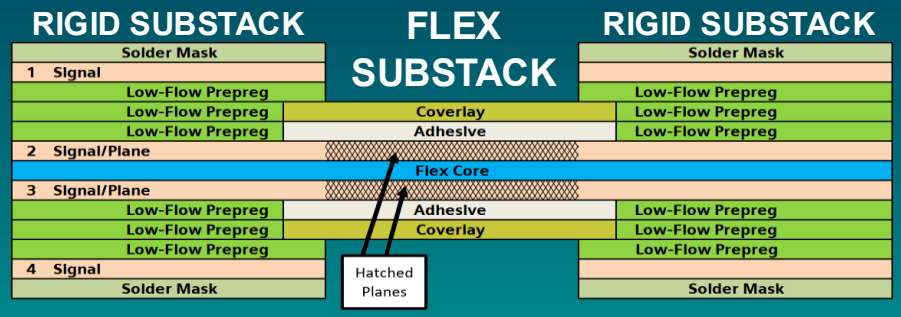
- Extensive material library makes it easy to make real designs
- Make design improvements with real materials

Stackup Comparison and Validation

- Compare Spec vs. Fabricator stackups
- Evaluate materials for any parameter
- Run manufacturing and SI checks



	A	B	C	D	E	F	G	H
	Category	Manufacturer	Material Name	Type	Construction	H (mils)	Resin (%)	Description
1	Z-zero	AGC Nelco	Meteorwave 1000	Core	106	2.00	73.0%	
2	Z-zero	AGC Nelco	Meteorwave 1000	Core	1078	2.50	59.0%	
3	Z-zero	AGC Nelco	Meteorwave 1000	Core	1078	3.00	65.0%	
4	Z-zero	AGC Nelco	Meteorwave 1000	Core	2013	3.50	53.0%	
5	Z-zero	AGC Nelco	Meteorwave 1000	Core	2x106	4.00	73.0%	
6	Z-zero	AGC Nelco	Meteorwave 1000	Core	2x1035	4.00	68.0%	
7	Z-zero	AGC Nelco	Meteorwave 1000	Core	2116	4.00	46.0%	
8	Z-zero	AGC Nelco	Meteorwave 1000	Core	3313	4.00	56.0%	
9	Z-zero	AGC Nelco	Meteorwave 1000	Core	2116	5.00	55.0%	



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Copper Roughness and Signal Integrity

“10 Things You Need to Know”

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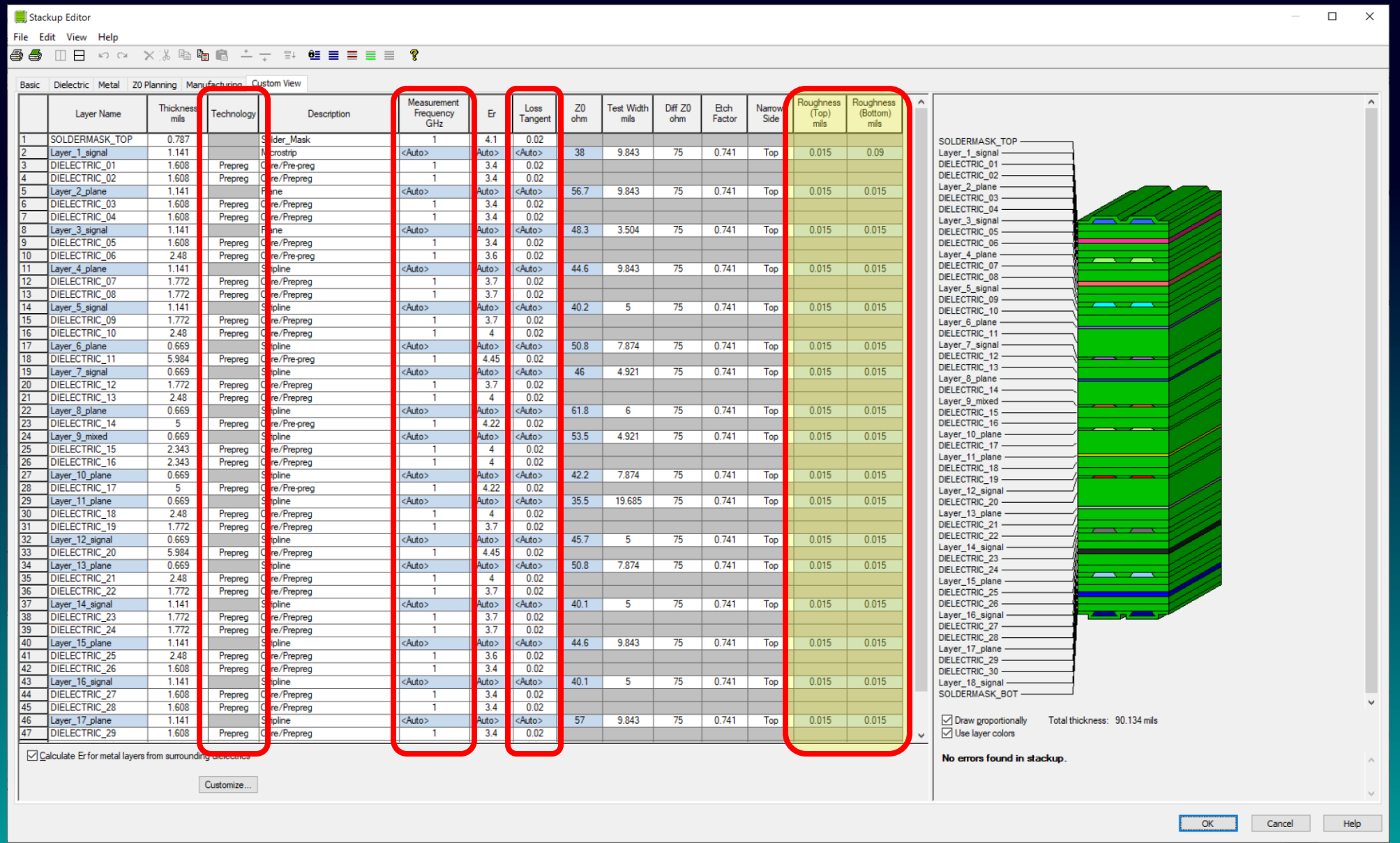
What's Wrong with this Picture?



	Layer Name	Thickness mils	Technology	Description	Measurement Frequency GHz	Er	Loss Tangent	Z0 ohm	Test Width mils	Diff Z0 ohm	Etch Factor	Narrow Side	Roughness (Top) mils	Roughness (Bottom) mils
1	SOLDERMASK_TOP	0.787		Solder_Mask	1	4.1	0.02							
2	Layer_1_signal	1.141		Microstrip	<Auto>	Auto>	<Auto>	38	9.843	75	0.741	Top	0.015	0.09
3	DIELECTRIC_01	1.608	Prepreg	Core/Pre-preg	1	3.4	0.02							
4	DIELECTRIC_02	1.608	Prepreg	Core/Prepreg	1	3.4	0.02							
5	Layer_2_plane	1.141		Plane	<Auto>	Auto>	<Auto>	56.7	9.843	75	0.741	Top	0.015	0.015
6	DIELECTRIC_03	1.608	Prepreg	Core/Prepreg	1	3.4	0.02							
7	DIELECTRIC_04	1.608	Prepreg	Core/Prepreg	1	3.4	0.02							
8	Layer_3_signal	1.141		Plane	<Auto>	Auto>	<Auto>	48.3	3.504	75	0.741	Top	0.015	0.015
9	DIELECTRIC_05	1.608	Prepreg	Core/Prepreg	1	3.4	0.02							
10	DIELECTRIC_06	2.48	Prepreg	Core/Pre-preg	1	3.6	0.02							
11	Layer_4_plane	1.141		Stripline	<Auto>	Auto>	<Auto>	44.6	9.843	75	0.741	Top	0.015	0.015
12	DIELECTRIC_07	1.772	Prepreg	Core/Prepreg	1	3.7	0.02							
13	DIELECTRIC_08	1.772	Prepreg	Core/Prepreg	1	3.7	0.02							
14	Layer_5_signal	1.141		Stripline	<Auto>	Auto>	<Auto>	40.2	5	75	0.741	Top	0.015	0.015
15	DIELECTRIC_09	1.772	Prepreg	Core/Prepreg	1	3.7	0.02							
16	DIELECTRIC_10	2.48	Prepreg	Core/Prepreg	1	4	0.02							
17	Layer_6_plane	0.669		Stripline	<Auto>	Auto>	<Auto>	50.8	7.874	75	0.741	Top	0.015	0.015
18	DIELECTRIC_11	5.984	Prepreg	Core/Pre-preg	1	4.45	0.02							
19	Layer_7_signal	0.669		Stripline	<Auto>	Auto>	<Auto>	46	4.921	75	0.741	Top	0.015	0.015
20	DIELECTRIC_12	1.772	Prepreg	Core/Prepreg	1	3.7	0.02							
21	DIELECTRIC_13	2.48	Prepreg	Core/Prepreg	1	4	0.02							
22	Layer_8_plane	0.669		Stripline	<Auto>	Auto>	<Auto>	61.8	6	75	0.741	Top	0.015	0.015
23	DIELECTRIC_14	5	Prepreg	Core/Pre-preg	1	4.22	0.02							
24	Layer_9_mixed	0.669		Stripline	<Auto>	Auto>	<Auto>	53.5	4.921	75	0.741	Top	0.015	0.015
25	DIELECTRIC_15	2.343	Prepreg	Core/Prepreg	1	4	0.02							
26	DIELECTRIC_16	2.343	Prepreg	Core/Prepreg	1	4	0.02							
27	Layer_10_plane	0.669		Stripline	<Auto>	Auto>	<Auto>	42.2	7.874	75	0.741	Top	0.015	0.015
28	DIELECTRIC_17	5	Prepreg	Core/Pre-preg	1	4.22	0.02							
29	Layer_11_plane	0.669		Stripline	<Auto>	Auto>	<Auto>	35.5	19.685	75	0.741	Top	0.015	0.015
30	DIELECTRIC_18	2.48	Prepreg	Core/Prepreg	1	4	0.02							
31	DIELECTRIC_19	1.772	Prepreg	Core/Prepreg	1	3.7	0.02							
32	Layer_12_signal	0.669		Stripline	<Auto>	Auto>	<Auto>	45.7	5	75	0.741	Top	0.015	0.015
33	DIELECTRIC_20	5.984	Prepreg	Core/Prepreg	1	4.45	0.02							
34	Layer_13_plane	0.669		Stripline	<Auto>	Auto>	<Auto>	50.8	7.874	75	0.741	Top	0.015	0.015
35	DIELECTRIC_21	2.48	Prepreg	Core/Prepreg	1	4	0.02							
36	DIELECTRIC_22	1.772	Prepreg	Core/Prepreg	1	3.7	0.02							
37	Layer_14_signal	1.141		Stripline	<Auto>	Auto>	<Auto>	40.1	5	75	0.741	Top	0.015	0.015
38	DIELECTRIC_23	1.772	Prepreg	Core/Prepreg	1	3.7	0.02							
39	DIELECTRIC_24	1.772	Prepreg	Core/Prepreg	1	3.7	0.02							
40	Layer_15_plane	1.141		Stripline	<Auto>	Auto>	<Auto>	44.6	9.843	75	0.741	Top	0.015	0.015
41	DIELECTRIC_25	2.48	Prepreg	Core/Prepreg	1	3.6	0.02							
42	DIELECTRIC_26	1.608	Prepreg	Core/Prepreg	1	3.4	0.02							
43	Layer_16_signal	1.141		Stripline	<Auto>	Auto>	<Auto>	40.1	5	75	0.741	Top	0.015	0.015
44	DIELECTRIC_27	1.608	Prepreg	Core/Prepreg	1	3.4	0.02							
45	DIELECTRIC_28	1.608	Prepreg	Core/Prepreg	1	3.4	0.02							
46	Layer_17_plane	1.141		Stripline	<Auto>	Auto>	<Auto>	57	9.843	75	0.741	Top	0.015	0.015
47	DIELECTRIC_29	1.608	Prepreg	Core/Prepreg	1	3.4	0.02							

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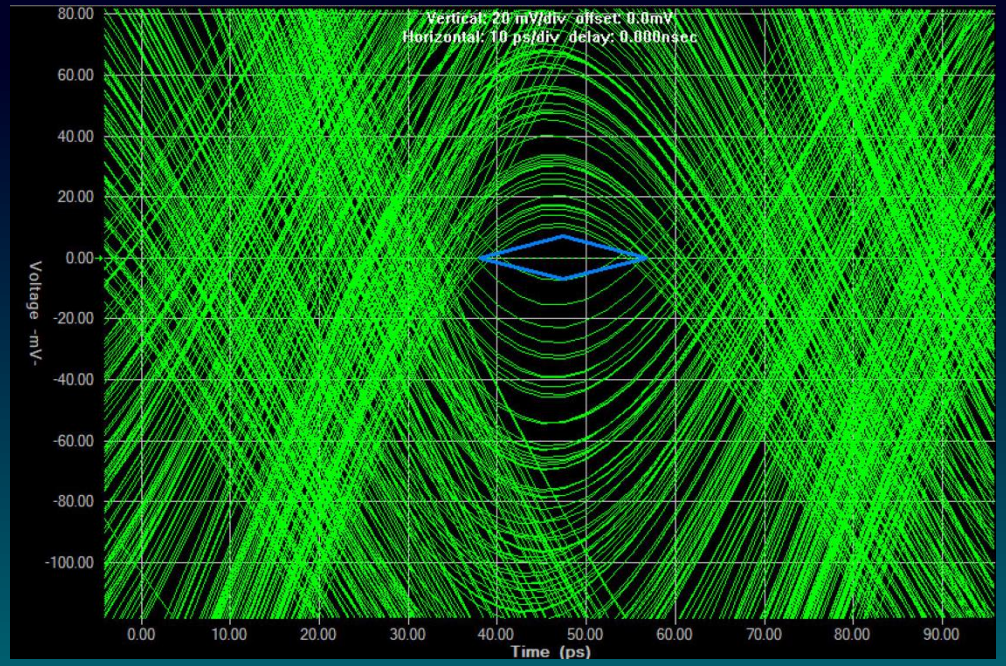
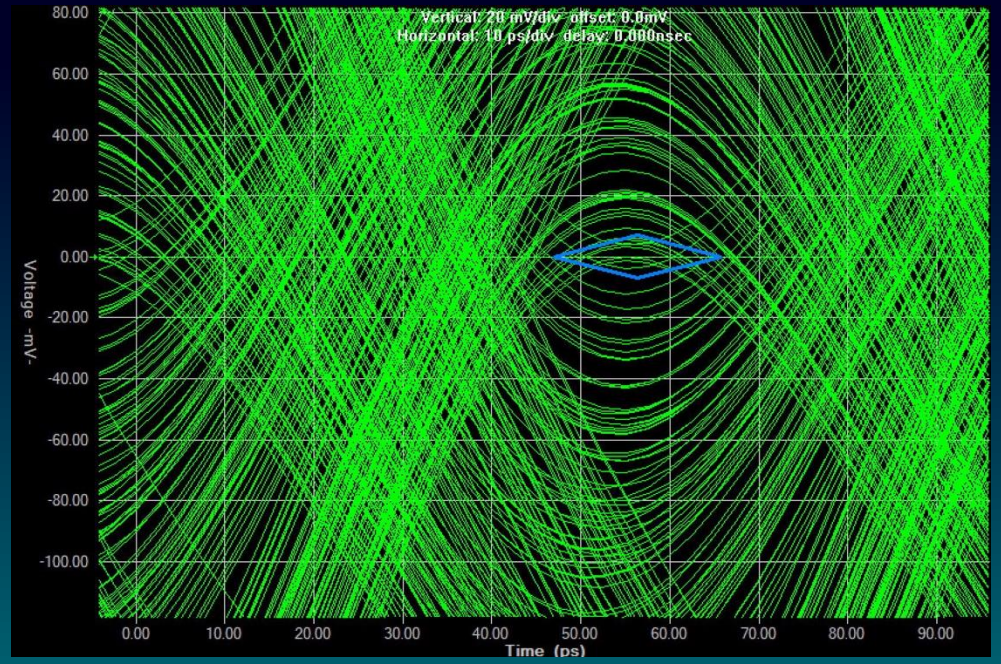
Why Do We Care?

The difference



Eye is right on the edge of the eye mask



Bit errors from rougher copper

- Same resin system
- **Different copper roughness**

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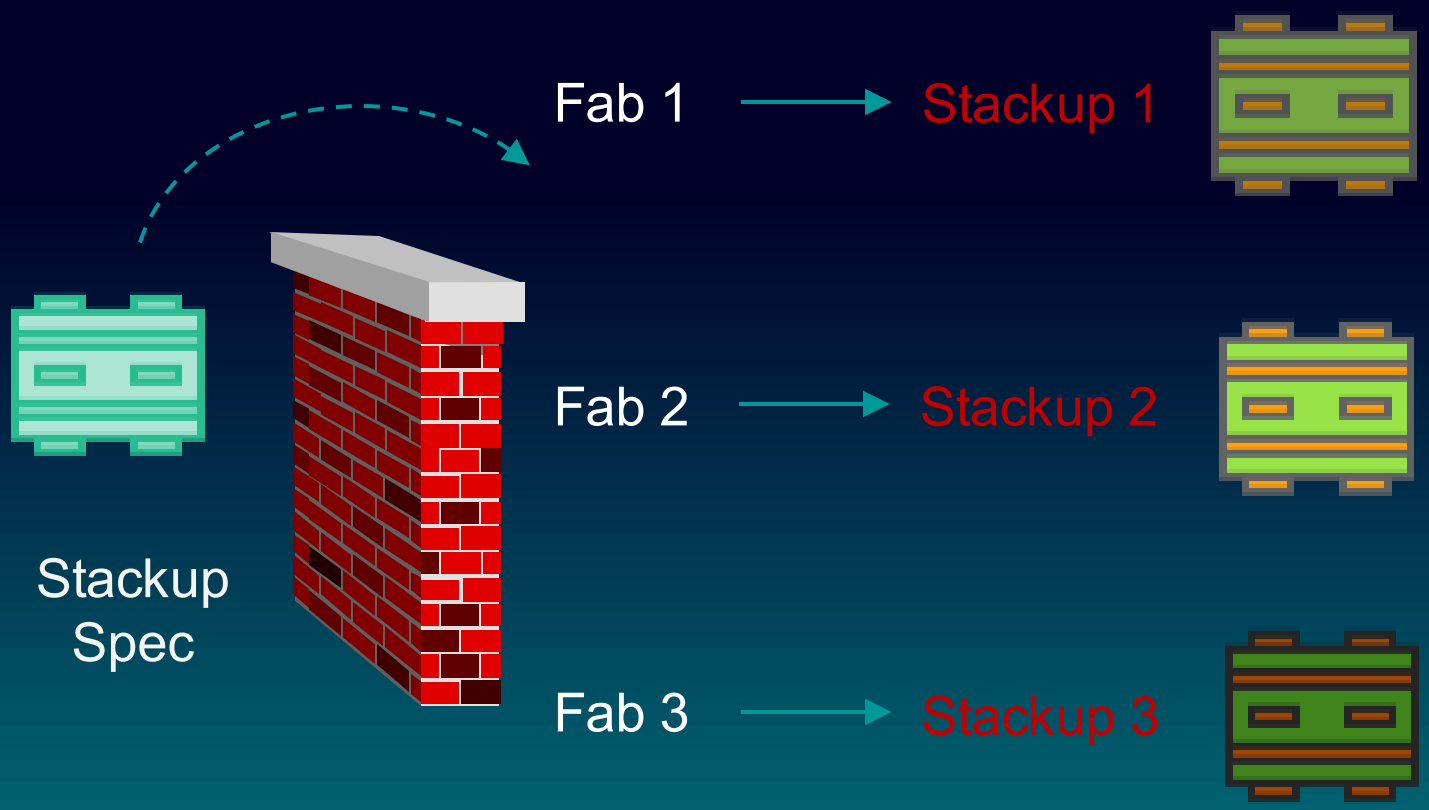
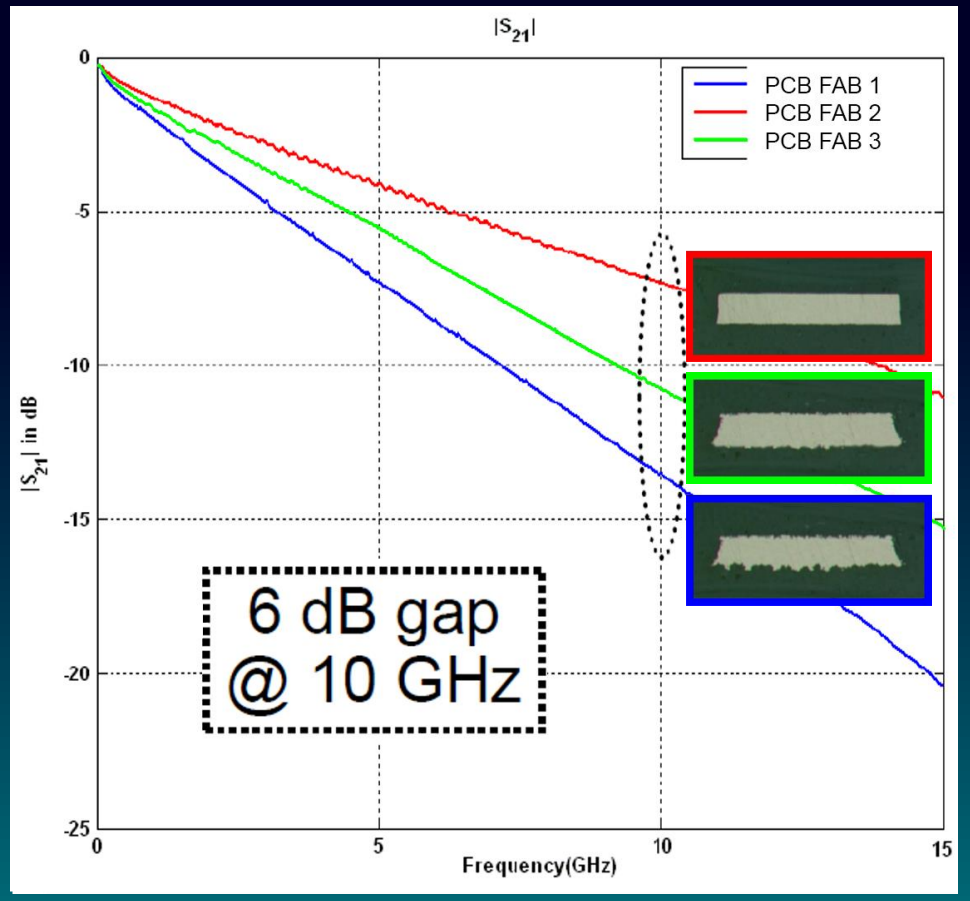
OEM

THREE FABRICATORS

THREE STACKUPS





Copper Roughness Needs to be Tracked across Every Fabricator

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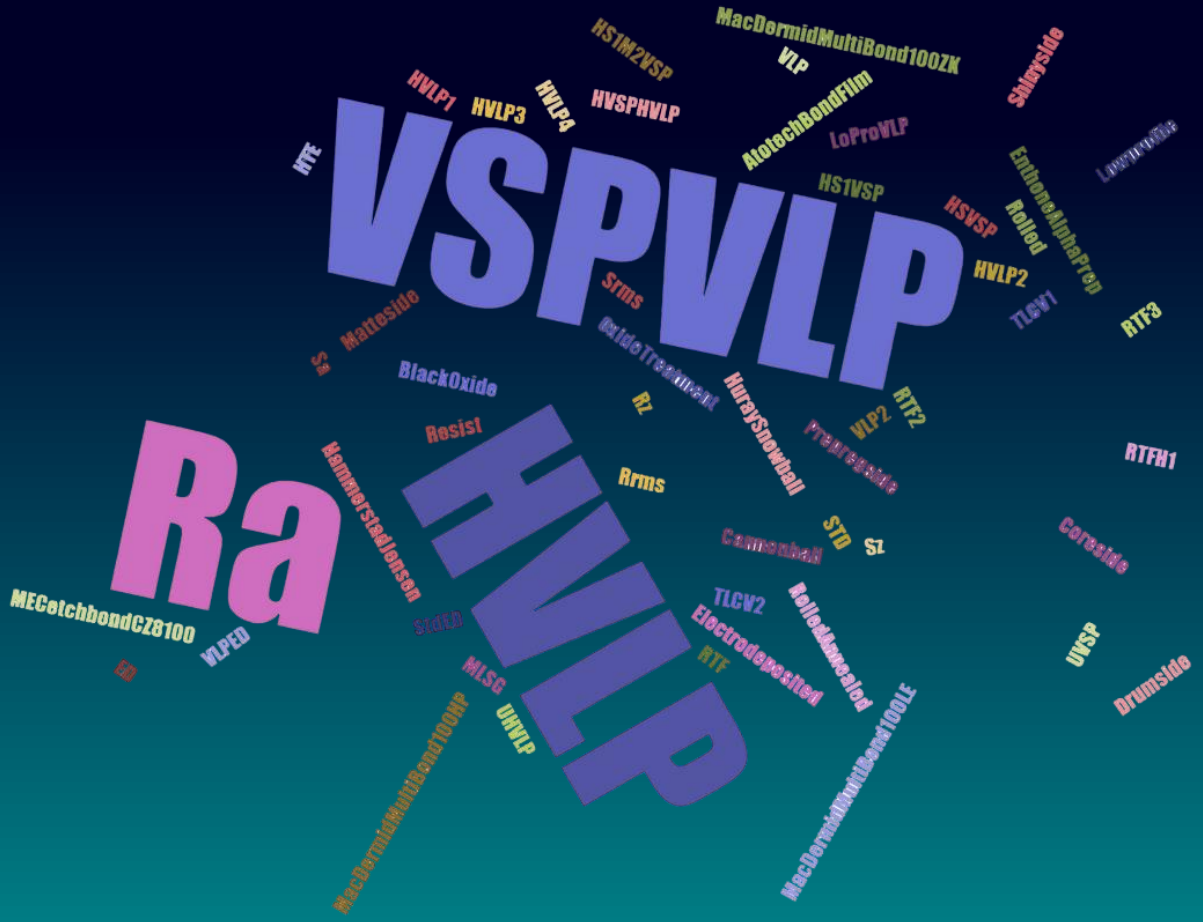
Tracking Copper Roughness - deli sürüsüne çobanlık



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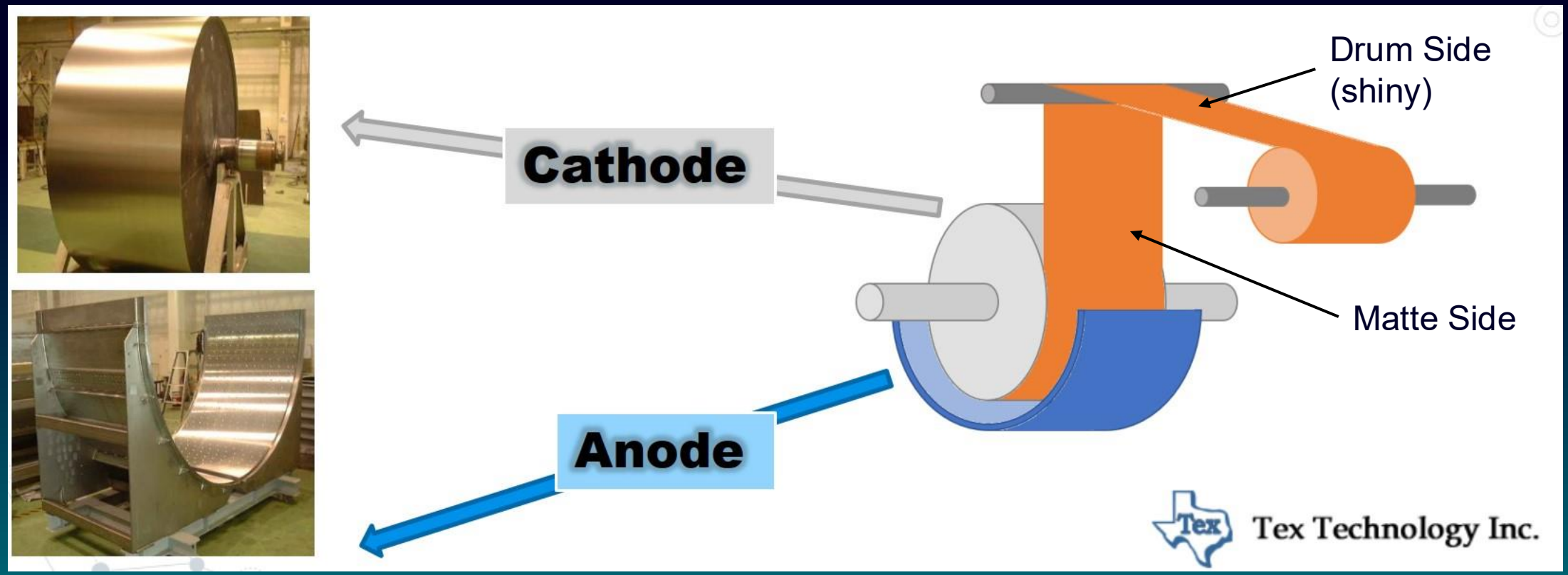
Electrodeposited Copper Foil Fabrication Process



Matte side typically has a different roughness than the drum side

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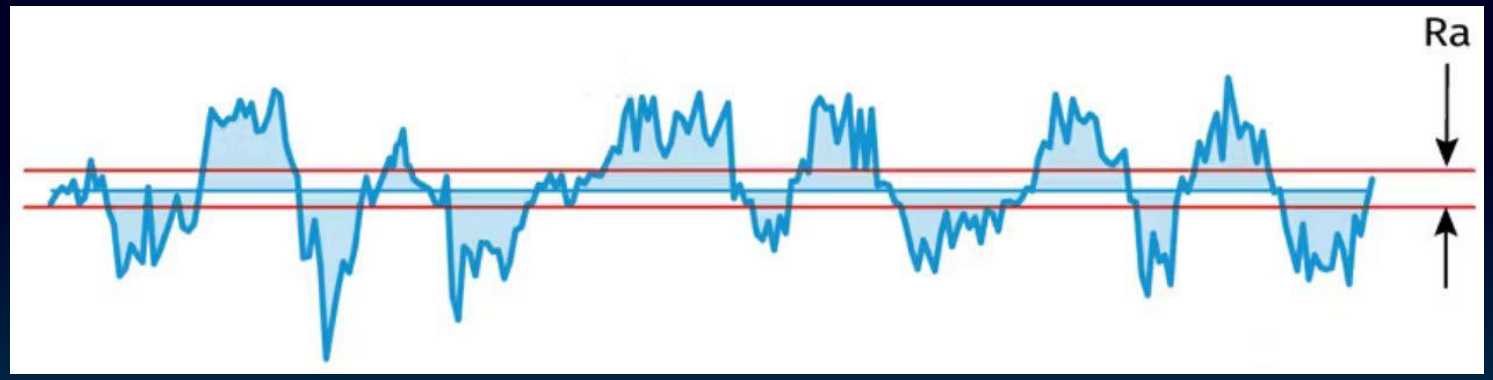
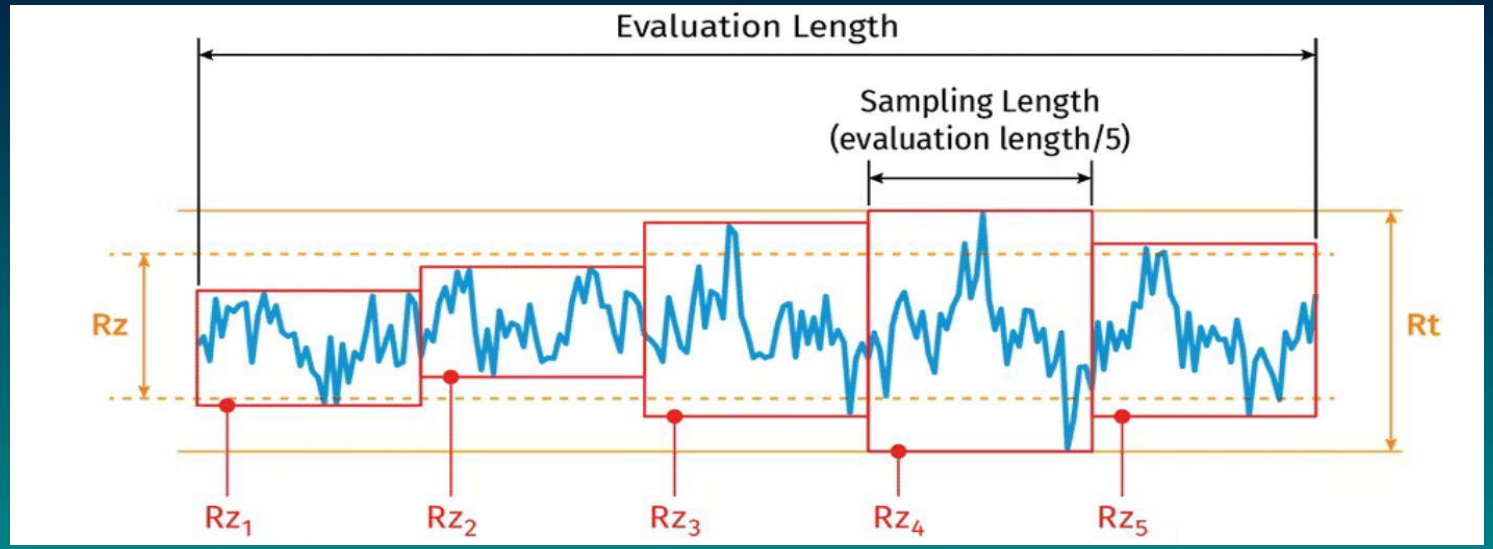
Common Measures for Surface Roughness - Ra and Rz



Average (Ra)

$$Ra = (1/L)\int_{o}^{L} |Z(x)|dx$$



10-point Mean (Rz)

$$Rz = \frac{|Yp_1+Yp_2+Yp_3+Yp_4+Yp_5|+|Yv_1+Yv_2+Yv_3+Yv_4+Yv_5|}{5}$$

$Yp_1, Yp_2, Yp_3, Yp_4, Yp_5$: Tallest 5 peaks within sample

$Yv_1, Yv_2, Yv_3, Yv_4, Yv_5$: Lowest 5 peaks within sample

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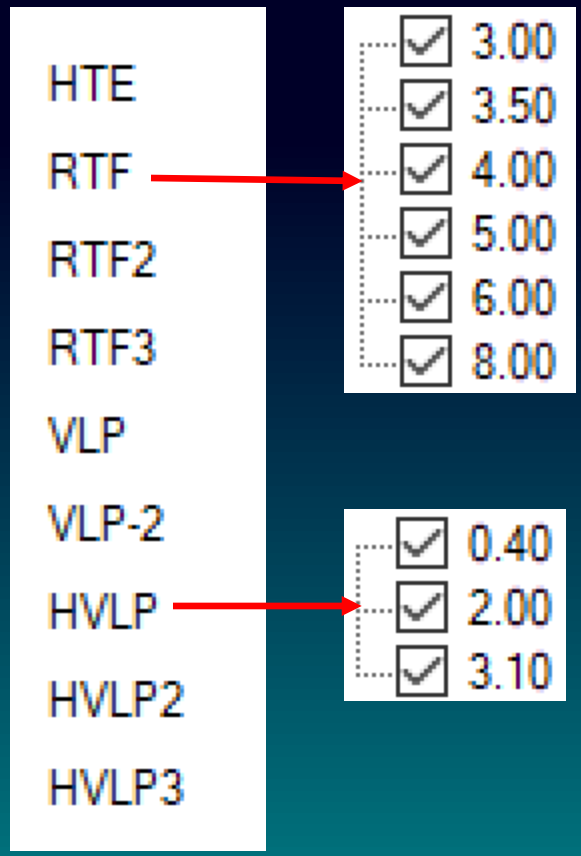
No Firm Standards for Designating Copper Foil Grades or Roughness

- There are several generic designations, but each copper supplier uses these terms differently
- No progress toward development of a solid roughness standard
- The only reliable way to control copper roughness today:
  - Find out what the laminate manufacturers offer (by foil name, copper roughness, and cost)
  - Simulate to make sure that it will meet your insertion loss goals
  - Include this in your stackup specification



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Two Sides to Track

- The core side is what most people think of when selecting copper foils
- Knowing the prepreg side is important, but more challenging
  - Rougher surface = stronger bond

Prepreg side is textured by the copper foil maker, plus … the PCB fabricator applies an oxide coating to top and side surfaces to maintain bond strength

(different options; see next slide)

Laminate side is textured by the copper foil maker who supplies the laminate vendor

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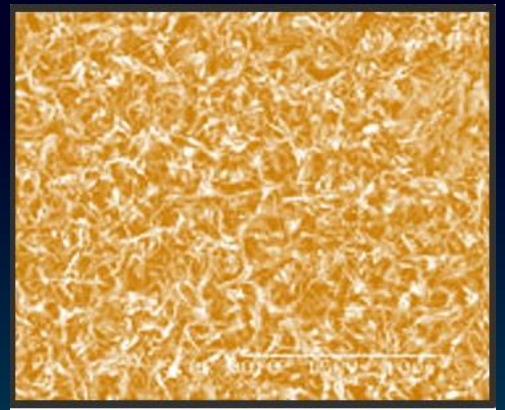
Industry-Standard Processes

- Oxide example:
  - Non-Proprietary Reduced Black Oxide (0 microns)
- Oxide alternative (OA) treatments:
  - MacDermid MultiBond 100LE (0.5-1.0 microns)**
  - Enthone Alpha-Prep (0.9-1.1 microns)**
  - MacDermid MultiBond 100ZK (1.0-1.5 microns)**
  - Atotech BondFilm (1.2-1.5 microns)**
  - MECetchbond CZ-8100 (1.5-2.0 microns)**
  - MacDermid MultiBond 100HP (2.5-4.0 microns)**

Increasing roughness

OA treatments can have a significant impact on electrical performance



Black Oxide at x5K

The proprietary products are technically "oxide alternatives" rather than true oxides.
They texturize the Cu surface rather than forming an oxide layer. True black oxide builds CuO crystal structure up from the copper surface; it's nonconductive and so carries no skin current. The others etch down into the Cu surface, thus texturing the Cu itself, and so DO affect skin current.

** Target values chosen by the PCB shop through selection of operating parameters (chemical concentration, temperature and line speed)

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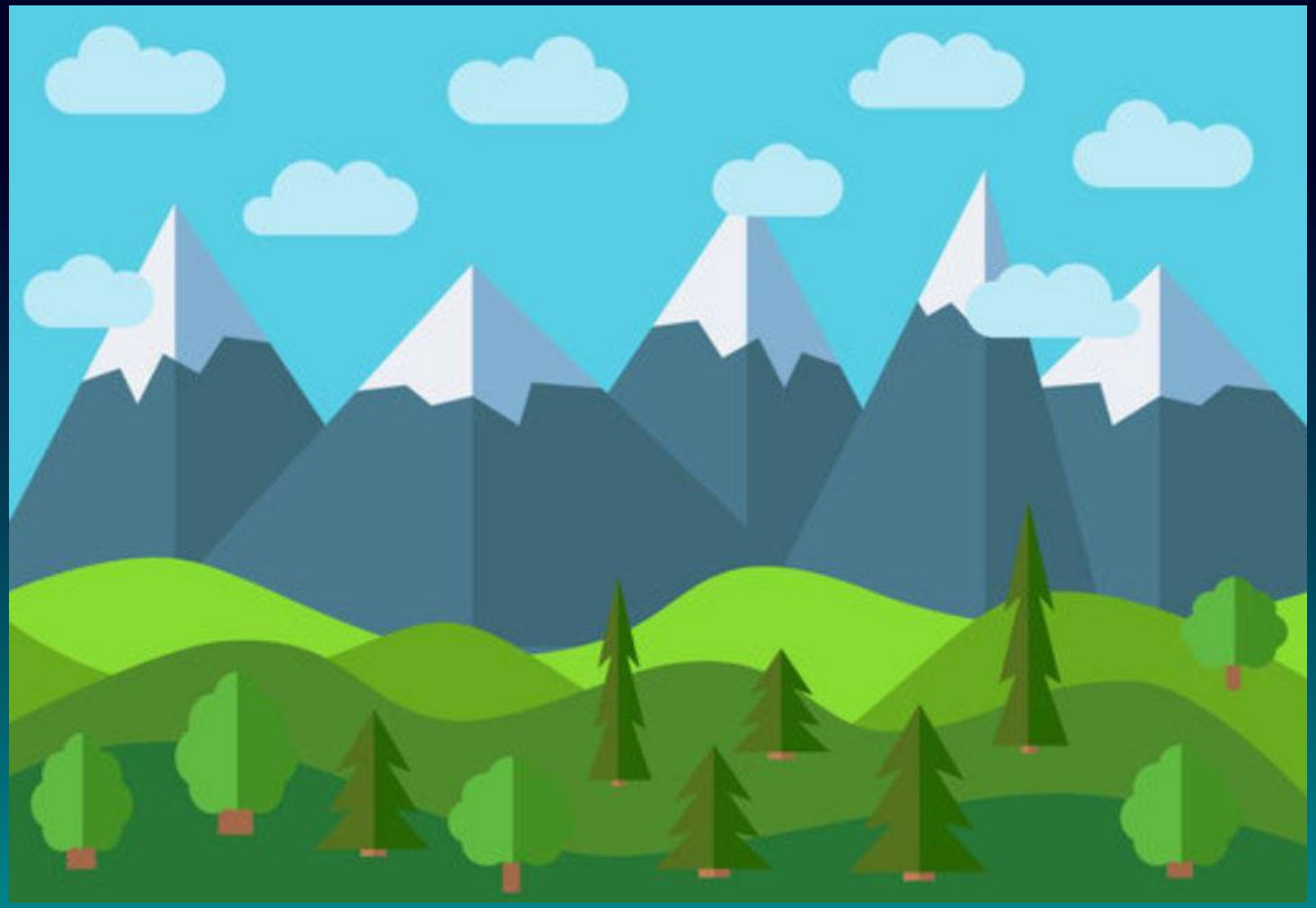
Base Copper Foil Selection vs. Process Treatments

Major differences are due to foil type (the mountains)

Minor differences due to process treatment type (the trees)



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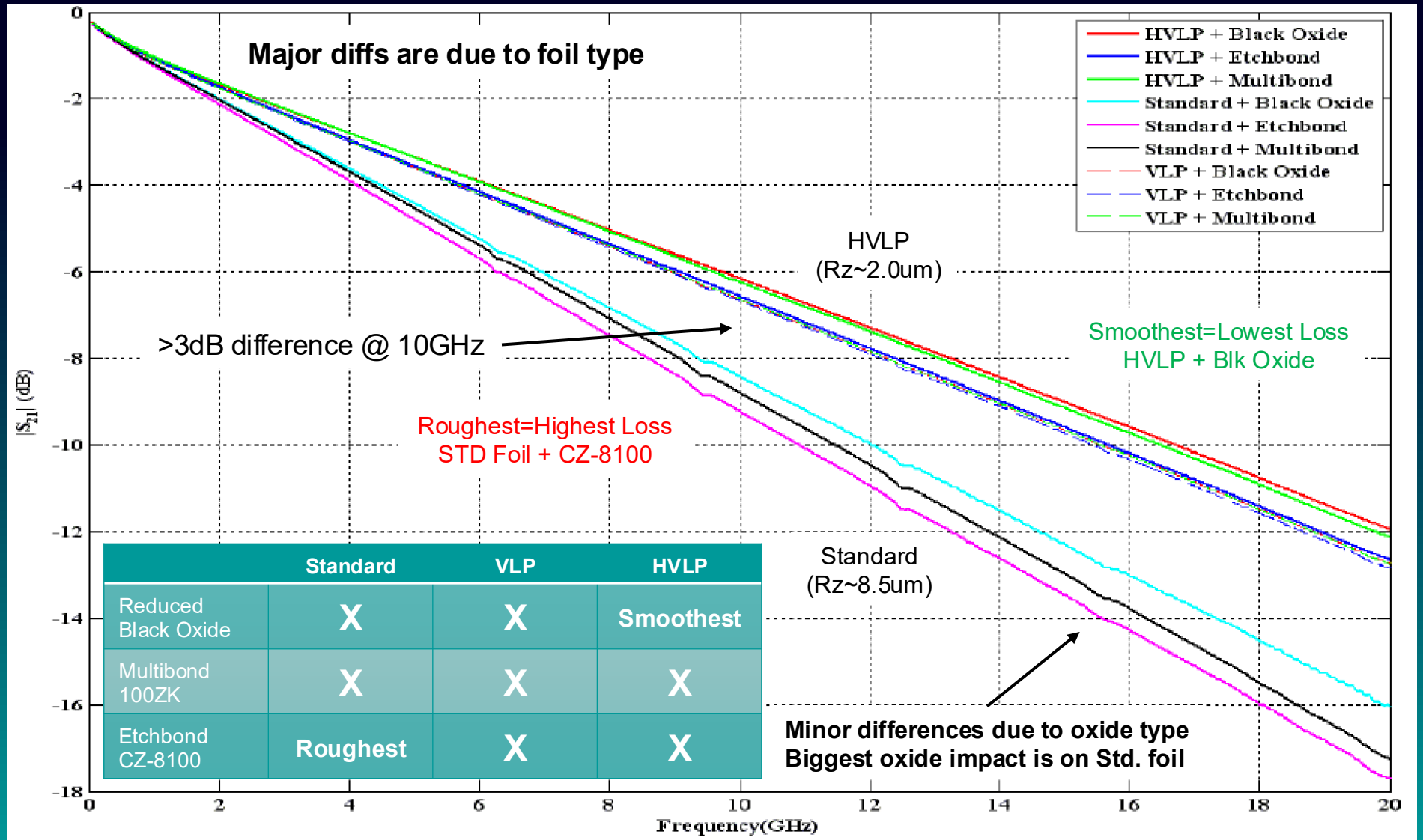
Copper Foil Selection has the Biggest Impact on Loss

(As compared to process treatments)



	Standard	VLP	HVLP
Reduced Black Oxide	X	X	Smoothest
Multibond 100ZK	X	X	X
Etchbond CZ-8100	Roughest	X	X

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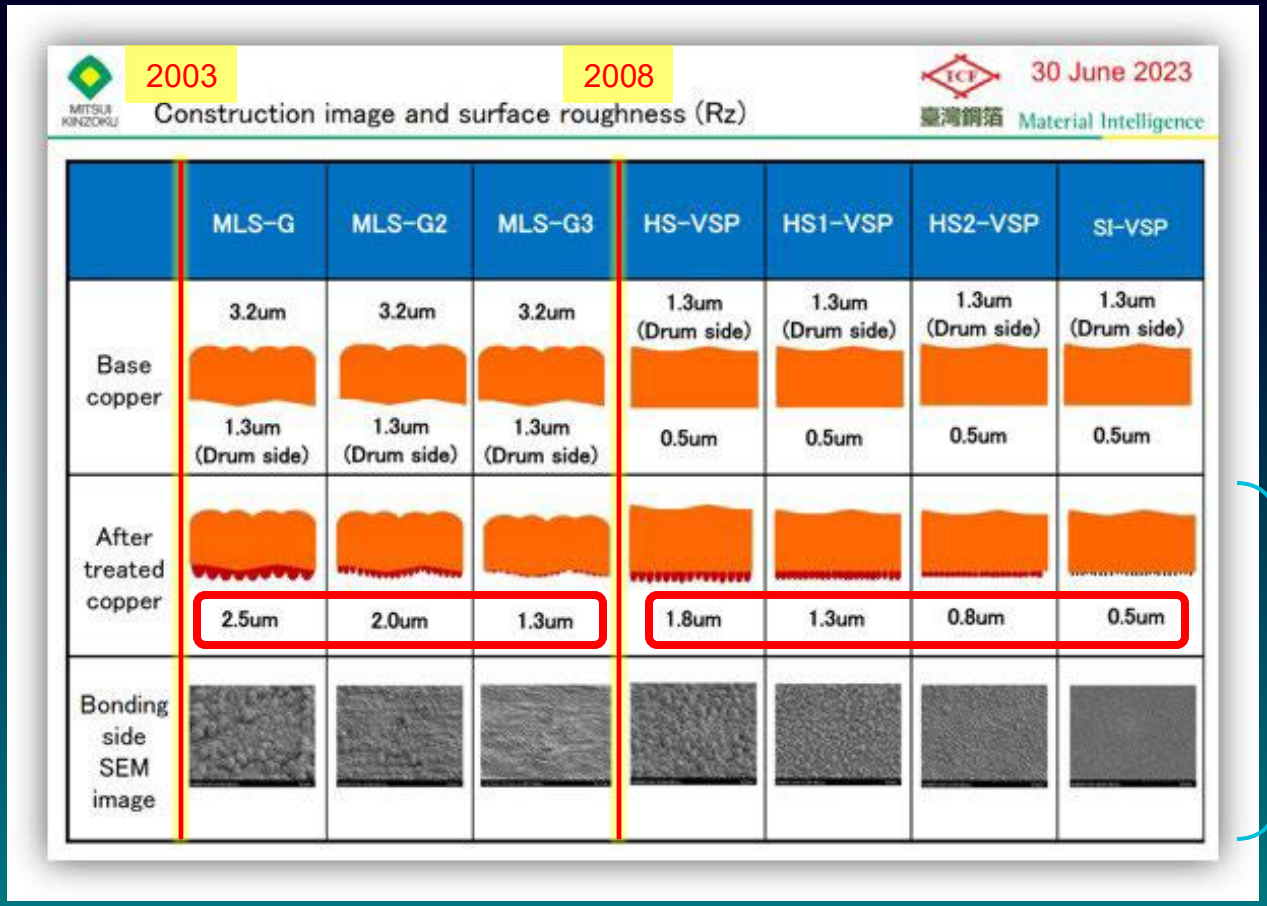
The Evolution of Copper Foils for High-Speed Applications

1. Prior to ~2003, laminate manufacturers had the rougher matte side of the copper facing the core side for better adhesion
2. With the advent of multi-Gbps SERDES signaling CCL vendors began flipping the smoother drum side down, commonly called RTF or “reverse-treated foil”. Over time, RTF nodulization treatments became smoother, but the rougher matte side remained
3. Then the smoother drum side was flipped back to face the prepreg side as Cu manufacturers developed smoother matte-side processes VLP nodulization treatments have become smoother with time (HVLP)



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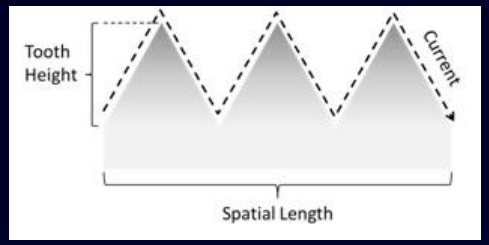
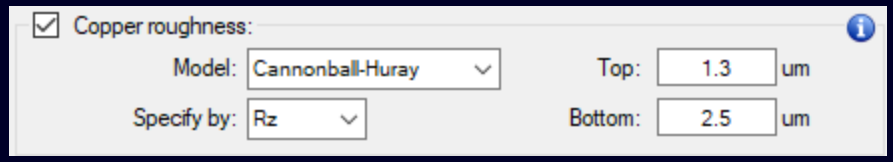
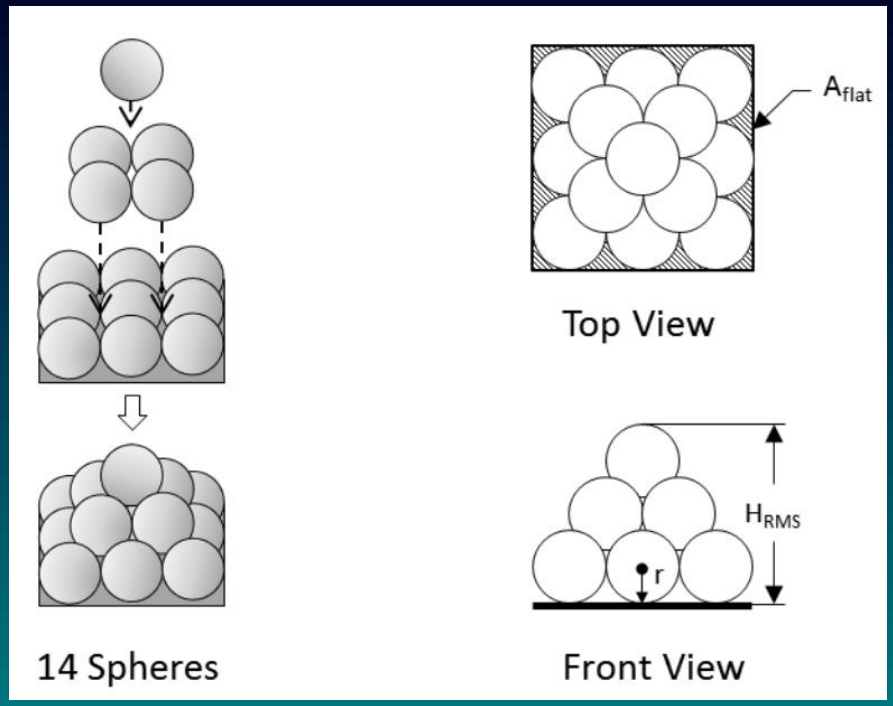
Different Models for Copper Roughness

- Hammerstad-Jensen
  - Sawtooth model
  - Loss saturates at ~5 GHz
- Huray Snowball
  - Theoretically, you can build an accurate “snowball model” of surface roughness through detailed analysis of SEM photographs
- Cannonball model
  - Three rows of equal spheres stacked on a square tile base
  - The radius of the spheres and tile area from the Huray model are determined solely by roughness parameters published in data sheets (e.g., Rz or Ra)
  - Can be used to practically represent the roughness/surface area, which is proportional to loss







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Z-planner Tracks and Models Roughness of Copper Foils

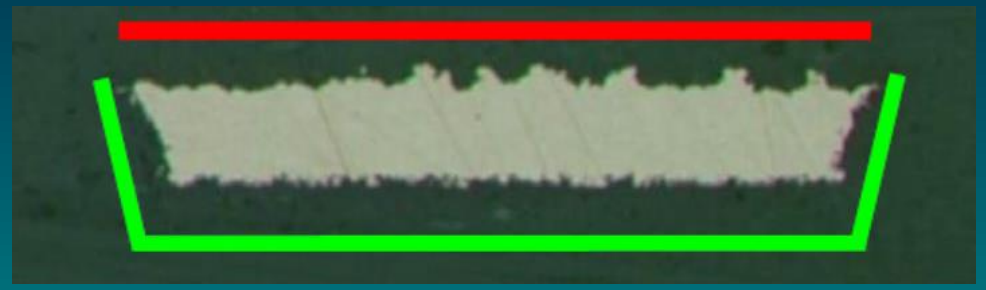
- Z-planner manages, tracks and models copper roughness and loss on both sides of copper foils

Raw aterial ickness (um)	Fab Finished Thickness (um)	Plane Type	Copper Foil	Etch Factor	Rz-Top (um)	Rz-Bottom (um)	Zo~ 5 Fat Widt
	12.7						
	30.5				3.0		
	15.2		HTE	**0.16**	7.5	7.5	2
37.2	**135.6**						
	15.2	Ground					
52.4	152.4						
	61.0	Power					
37.2	**125.0**						
	61.0	Power					
52.4	152.4						
	15.2	Ground					

HTE
RTF
RTF2
RTF3
VLP
VLP2
HVLP
HVLP2
HVLP3
PVLP
FVLP

Copper foil selection in Stackup View

Core



Prepreg

Library View (Core-side Rz)

AO	AP	AQ	AR	AS	AT	AU	AV
Primary Copper	Primary Cu Rz (um)	Secondary Copper	Secondary Cu Rz (um)	Tertiary Copper	Tertiary Cu Rz (um)	Quartenary Copper	Quartenary Cu Rz (um)
HVLP	2.00	HVLP2	1.50	HVLP3	1.00	HVLP4	0.80
HVLP	2.00	HVLP2	2.00	HVLP3	2.00	HVLP4	1.50

Library View (Prepreg-side Rz)

4 different Cu options for this laminate

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Z-planner Tracks and Models Roughness for Plating and Sequential Lamination

Sequential Lamination

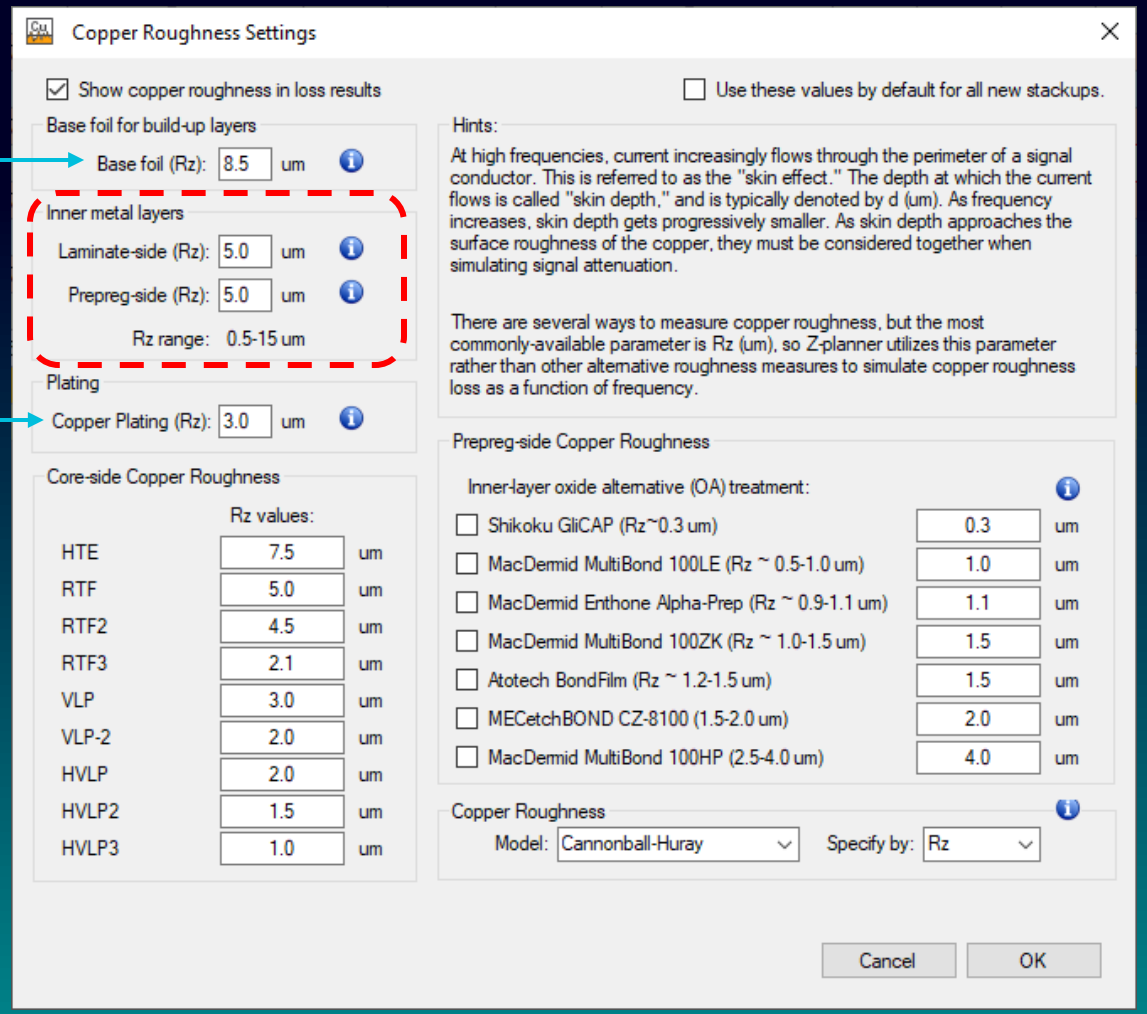
- “Build-up layers” are added by the PCB mfgr.
- So the copper foils are off the PCB fab’s shelves
- They typically use “HTE“ copper foils because they’re rough and have good peel strength
- Default roughness (Rz) is 8.5um
- High-speed boards might theoretically use smoother copper by special request

Plating

- Has its own unique roughness
- Research says Rz~3um is a good value

Rules for prepreg-side roughness

- If the laminate manufacturer has given us a prepreg-side roughness for a specific foil grade, we use that (Rz) number facing the prepreg
- If we don’t have that number, we use the core-side roughness for the prepreg from the laminate manufacturer
- If we don’t have either of the above, we use these generic (but reasonable) values



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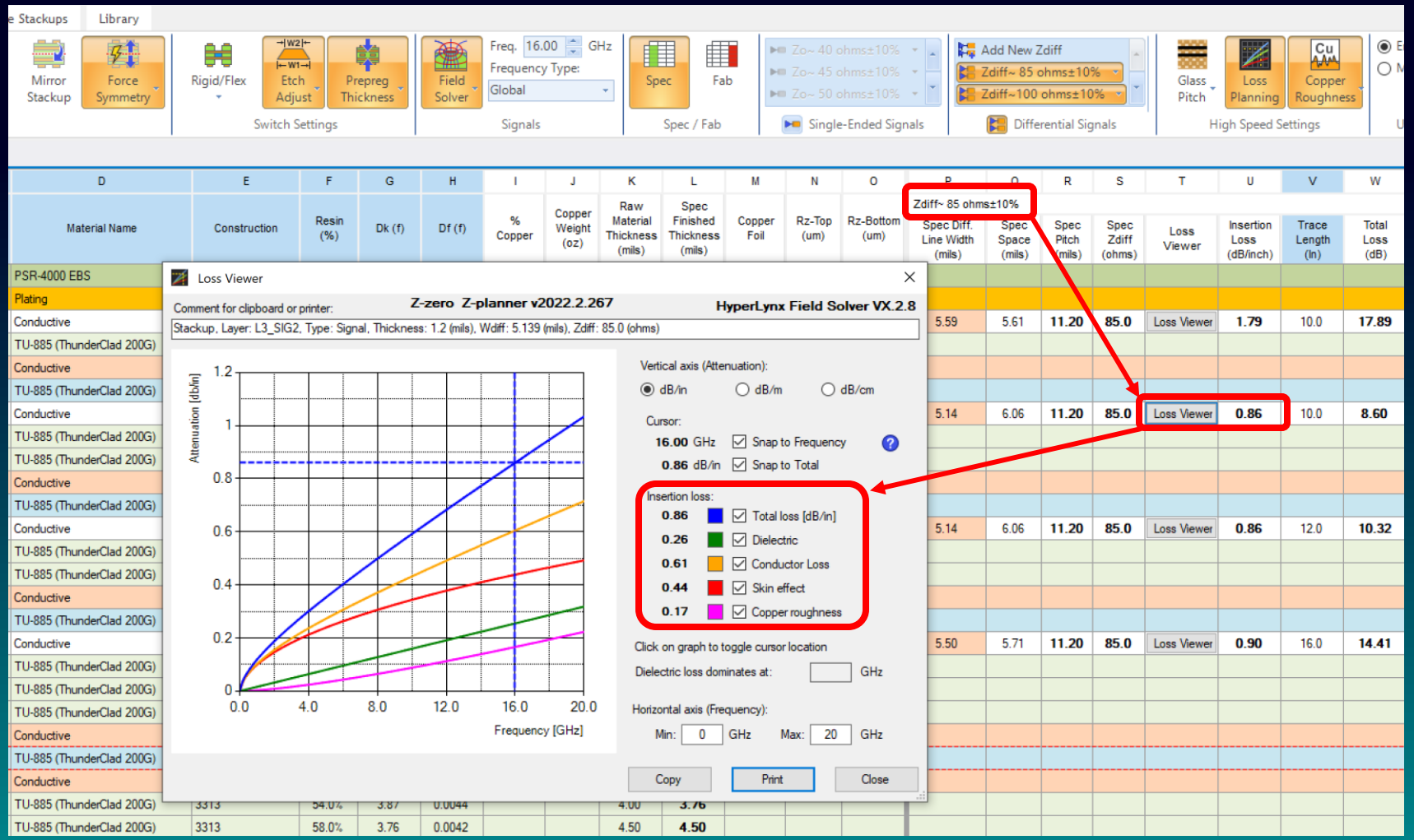
Detailed Insertion-Loss Modeling in Z-planner

- Z-planner uses real materials with data from the laminate vendors
- This shows TU-885, targeting PCIe 5.0) loss requirements, including Dk and Df as a function of frequency and resin content
- Copper foils/roughness modeled on both sides



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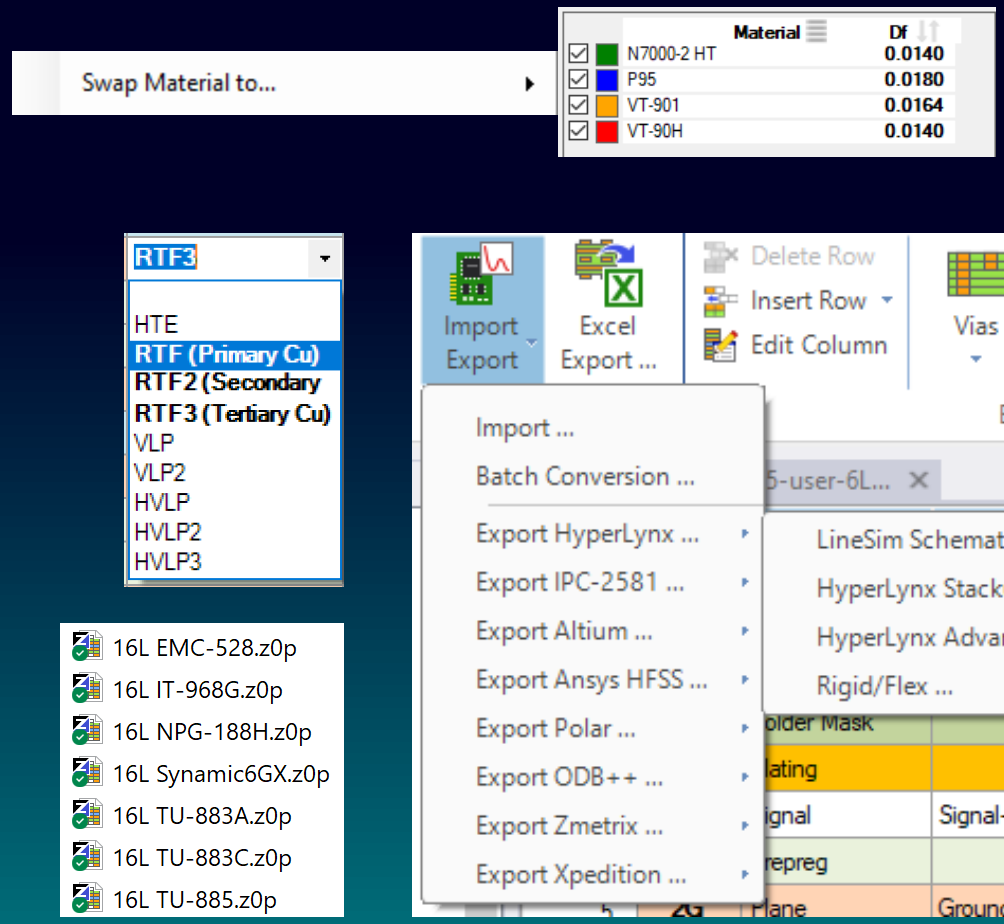
Easily Check all Materials being Considered

- Right click on a dielectric and redesign the whole stackup to another material to simulate loss performance
- Explore copper roughness options and recalculate insertion loss
- Export to HyperLynx – for signoff and whole board simulation
- Faster and much less expensive than taking 6 months to build and measure Signal Integrity Test Vehicles (SITVs) and tens of thousands of dollars



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Improvements to the Earlier Stackup

Stackup Editor

File Edit View Help

Basic | Dielectric | Metal | Z0 Planning | Manufacturing | Custom View

	Layer Name	Thickness mils, oz	Technology	Description	Measurement Frequency GHz	Er	Loss Tangent	Z0 ohm	Test Width mils	Target Z0 ohm	Etch Factor	Narrow Side	Roughness (Top) mils	Roughness (Bottom) mils
1	SOLDERMASK_TOP	0.787		THP-100 DX1 GF (Editable)	10	4.1	0.012							
2	Layer_1_signal	0.889		Microstrip	10	4.1	0.012	44.5	9.016	72.4	0.425	Top	0.097	0.097
3	DIELECTRIC_01	2	Prepreg	TU-872 LK (1067) RC=66%	10	3.4	0.0091							
4	DIELECTRIC_02	1.88	Prepreg	TU-872 LK (1067) RC=66%	10	3.4	0.0091							
5	Layer_2_plane	0.889		Plane	10	2.72	0.01365	100.6	1.2	75	0.3333	Top	0.045	0.097
6	DIELECTRIC_03	2	Prepreg	TU-872 LK (1067) RC=66%	10	3.4	0.0091							
7	DIELECTRIC_04	1.1	Prepreg	TU-872 LK (1067) RC=66%	10	3.4	0.0091							
8	Layer_3_signal	0.889		Plane	10	2.72	0.01365	37.1	5.984	67.1	0.425	Top	0.045	0.097
9	DIELECTRIC_05	2	Prepreg	TU-872 LK (1067) RC=66%	10	3.4	0.0091							
10	DIELECTRIC_06	2.88	Prepreg	TU-872 LK (1078) RC=63%	10	3.47	0.009							
11	Layer_4_plane	0.889		Stripline	10	2.776	0.0135	90.8	1.2	75	0.3333	Top	0.045	0.097
12	DIELECTRIC_07	2.2	Prepreg	TU-862 HF (106) RC=74.0%	10	3.69	0.0192							
13	DIELECTRIC_08	1.3	Prepreg	TU-862 HF (106) RC=74.0%	10	3.69	0.0192							
14	Layer_5_signal	0.889		Stripline	10	2.952	0.0288	37.2	5.984	66.9	0.425	Top	0.045	0.097
15	DIELECTRIC_09	2.2	Prepreg	TU-862 HF (106) RC=74.0%	10	3.69	0.0192							
16	DIELECTRIC_10	2.84	Prepreg	TU-862 HF (1080) RC=63%	10	4	0.0174							
17	Layer_6_plane	0.444		Stripline	10	3.2	0.0261	107.4	0.6	75	0.3333	Top	0.057	0.034
18	DIELECTRIC_11	6	Core	TU-862 HF (2x1080) H - H	10	3.97	0.0176							
19	Layer_7_signal	0.444		Stripline	10	3.2	0.0261	93.2	0.6	75	0.283	Bottom	0.034	0.057
20	DIELECTRIC_12	1.75	Prepreg	TU-862 HF (106) RC=74.0%	10	3.69	0.0192							
21	DIELECTRIC_13	2.84	Prepreg	TU-862 HF (1080) RC=63%	10	4	0.0174							
22	Layer_8_plane	0.444		Stripline	10	3.2	0.0261	109.5	0.6	75	0.3333	Top	0.057	0.034
23	DIELECTRIC_14	5	Core	TU-862 HF (2x1080) H - H	10	4.11	0.0168							
24	Layer_9_mixed	0.444		Stripline	10	3.2	0.0261	98.2	0.6	75	0.283	Bottom	0.034	0.057
25	DIELECTRIC_15	2.45	Prepreg	TU-862 HF (1080) RC=63%	10	4	0.0174							
26	DIELECTRIC_16	2.45	Prepreg	TU-862 HF (1080) RC=63%	10	4	0.0174							
27	Layer_10_plane	0.444		Stripline	10	3.2	0.0261	98.2	0.6	75	0.283	Top	0.057	0.034
28	DIELECTRIC_17	5	Core	TU-862 HF (2x1080) H - H	10	4.11	0.0168							
29	Layer_11_plane	0.444		Stripline	10	3.2	0.0261	109.5	0.6	75	0.3333	Bottom	0.034	0.057
30	DIELECTRIC_18	2.84	Prepreg	TU-862 HF (1080) RC=63%	10	4	0.0174							
31	DIELECTRIC_19	1.75	Prepreg	TU-862 HF (106) RC=74.0%	10	3.69	0.0192							
32	Layer_12_signal	0.444		Stripline	10	3.2	0.0261	93.2	0.6	75	0.283	Top	0.057	0.034
33	DIELECTRIC_20	6	Core	TU-862 HF (2x1080) H - H	10	3.97	0.0176							
34	Layer_13_plane	0.444		Stripline	10	3.2	0.0261	107.4	0.6	75	0.3333	Bottom	0.034	0.057
35	DIELECTRIC_21	2.84	Prepreg	TU-862 HF (1080) RC=63%	10	4	0.0174							
36	DIELECTRIC_22	2.2	Prepreg	TU-862 HF (106) RC=74.0%	10	3.69	0.0192							
37	Layer_14_signal	0.889		Stripline	10	2.952	0.0288	37.2	5.984	66.9	0.425	Bottom	0.097	0.097
38	DIELECTRIC_23	1.3	Prepreg	TU-862 HF (106) RC=74.0%	10	3.69	0.0192							
39	DIELECTRIC_24	2.2	Prepreg	TU-862 HF (106) RC=74.0%	10	3.69	0.0192							
40	Layer_15_plane	0.889		Stripline	10	2.776	0.0135	90.8	1.2	75	0.3333	Bottom	0.097	0.097
41	DIELECTRIC_25	2.88	Prepreg	TU-872 LK (1078) RC=63%	10	3.47	0.009							
42	DIELECTRIC_26	2	Prepreg	TU-872 LK (1067) RC=66%	10	3.4	0.0091							
43	Layer_16_signal	0.889		Plane	10	2.72	0.01365	37.1	5.984	67.1	0.425	Bottom	0.097	0.097
44	DIELECTRIC_27	1.1	Prepreg	TU-872 LK (1067) RC=66%	10	3.4	0.0091							

SOLDERMASK_TOP
Layer_1_signal
DIELECTRIC_01
DIELECTRIC_02
Layer_2_plane
DIELECTRIC_03
DIELECTRIC_04
Layer_3_signal
DIELECTRIC_05
DIELECTRIC_06
Layer_4_plane
DIELECTRIC_07
DIELECTRIC_08
Layer_5_signal
DIELECTRIC_09
DIELECTRIC_10
Layer_6_plane
DIELECTRIC_11
Layer_7_signal
DIELECTRIC_12
DIELECTRIC_13
Layer_8_plane
DIELECTRIC_14
Layer_9_mixed
DIELECTRIC_15
DIELECTRIC_16
Layer_10_plane
DIELECTRIC_17
Layer_11_plane
DIELECTRIC_18
DIELECTRIC_19
Layer_12_signal
DIELECTRIC_20
Layer_13_plane
DIELECTRIC_21
DIELECTRIC_22
Layer_14_signal
DIELECTRIC_23
DIELECTRIC_24
Layer_15_plane
DIELECTRIC_25
DIELECTRIC_26
Layer_16_signal
DIELECTRIC_27
DIELECTRIC_28
Layer_17_plane
DIELECTRIC_29
DIELECTRIC_30
Layer_18_signal

Draw proportionally Total thickness: 95.255 mils
Use layer colors

No errors found in stackup.

Calculate Er for metal layers from surrounding dielectrics

Customize...

OK Cancel Help

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Any questions?

anton.glinkin@cdtas.com

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