Designing without limits: the freedom of an integrated PCB Flow

Olivier ARNAUD – olivier.arnaud@siemens.com
Siemens EDA
Applications Engineer Consultant - ECC

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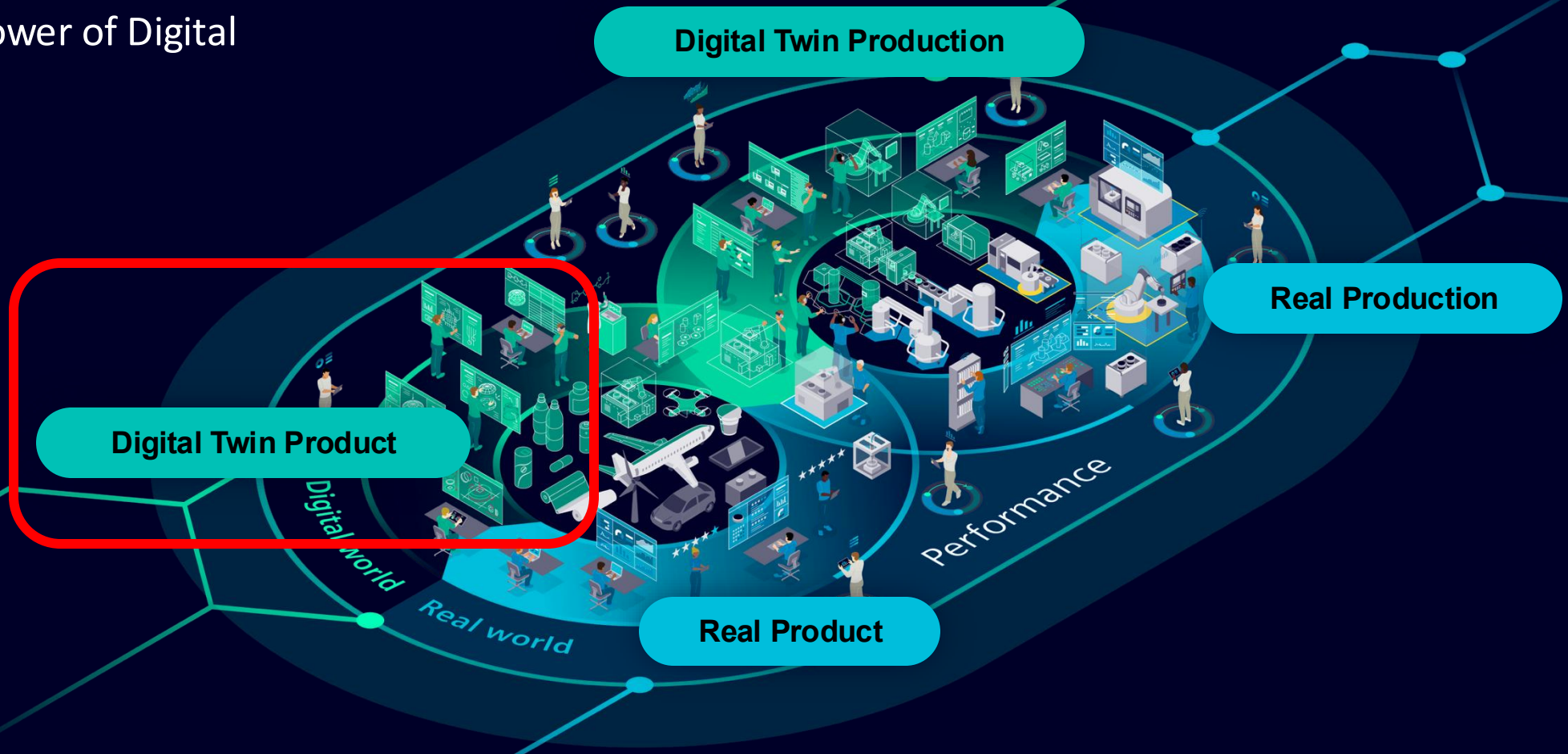
The digital twin concept revolutionizes how we design, develop, operate, and maintain complex systems and products

Accelerate Electronic Innovation with the Power of Digital



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A proactive approach for better results with integrated design solutions
The KPIs of best-in-class design

State-of-the-art design key focus areas

- Productivity through tool and process efficiency
- Unified design data management
- Simulation and analysis
- Multi-team collaboration

Aberdeen Group

What defines **“Best-in-Class”**

92% meet **product cost targets**

89% meet **launch dates**

94% meet **quality targets**

90% meet **revenue targets**

Industry average performance is 75% or lower in each category.

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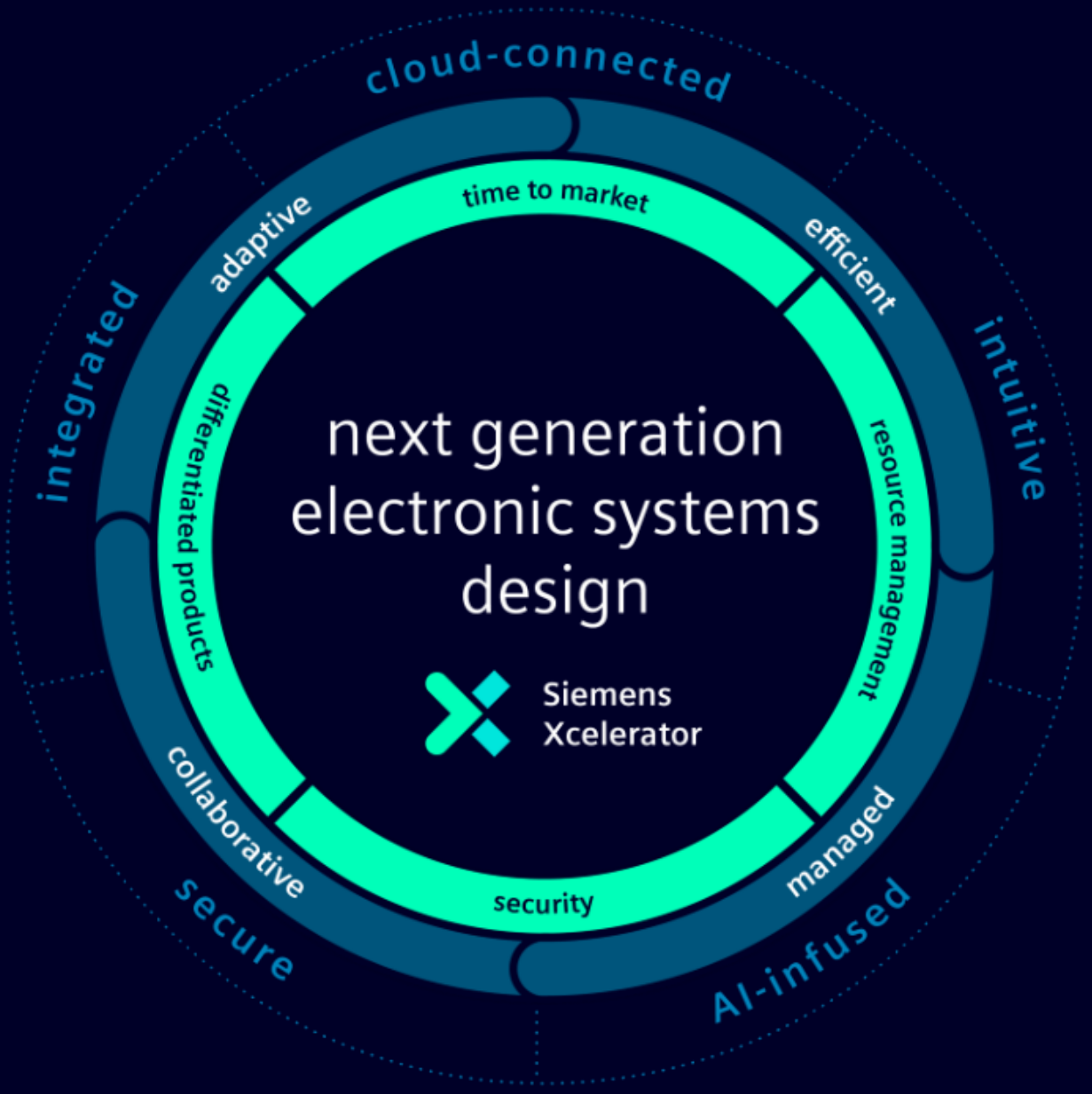
Next Generation Electronic Systems Design



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Removes the barriers of complexity, accelerates productivity, and delivers positive experiences for engineers and their teams

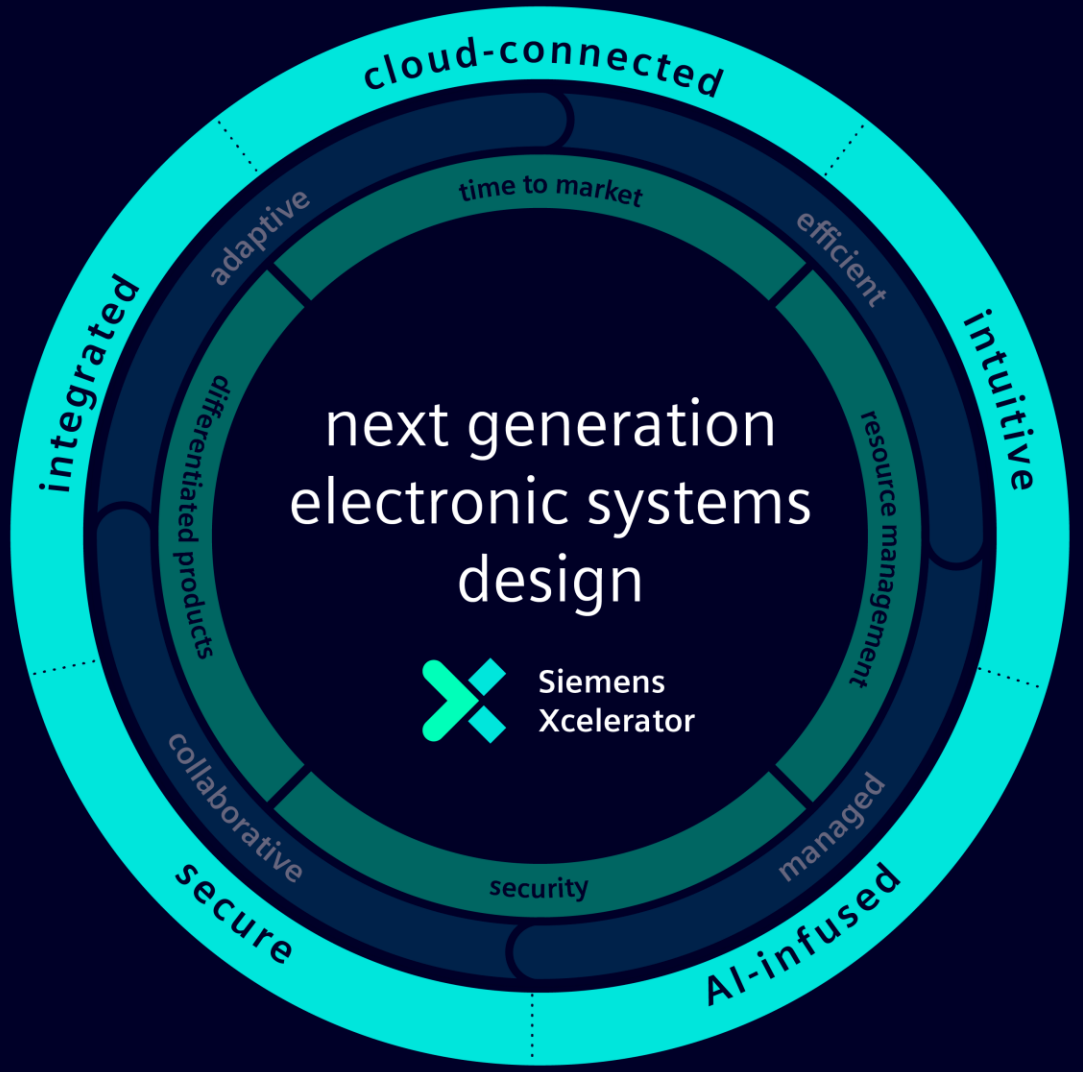
Intuitive
Boost productivity with a modern user experience

AI-infused
Accelerate design optimization and automation

Cloud-connected
Collaborate seamlessly across the ecosystem

Integrated
Leverage digital threads across multiple domains

Secure
Ensure the protection of critical design IP



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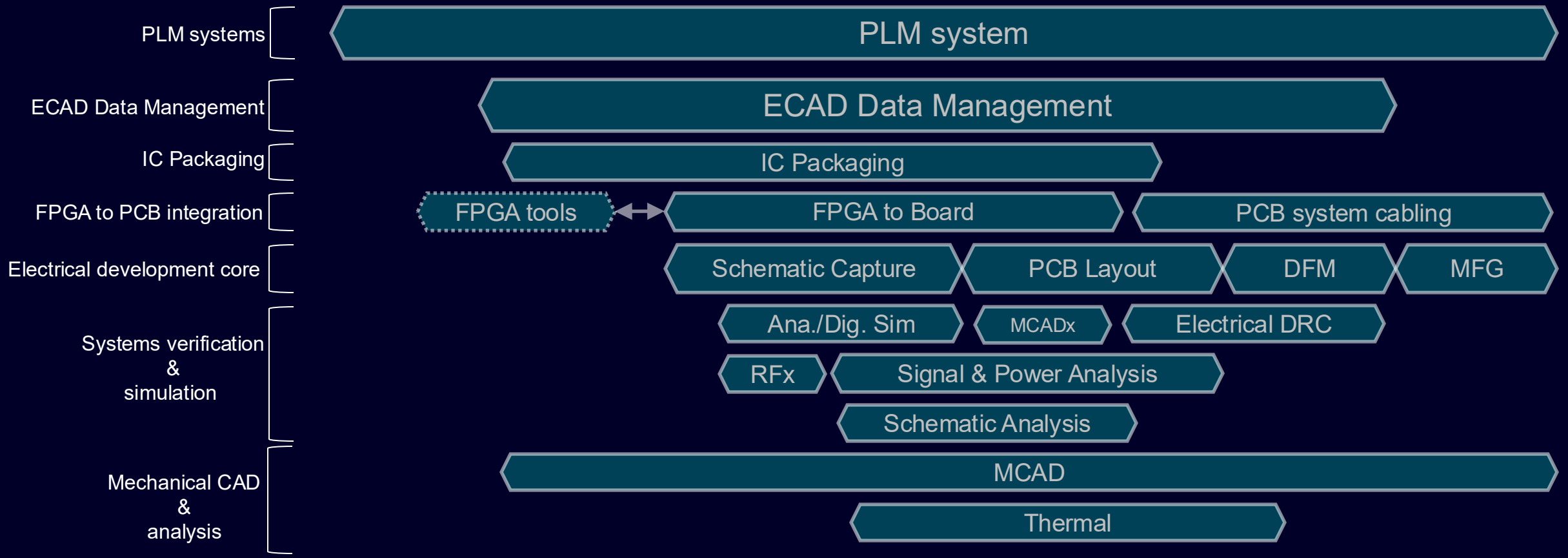
Digital Thread Critical Elements for ECAD System Design



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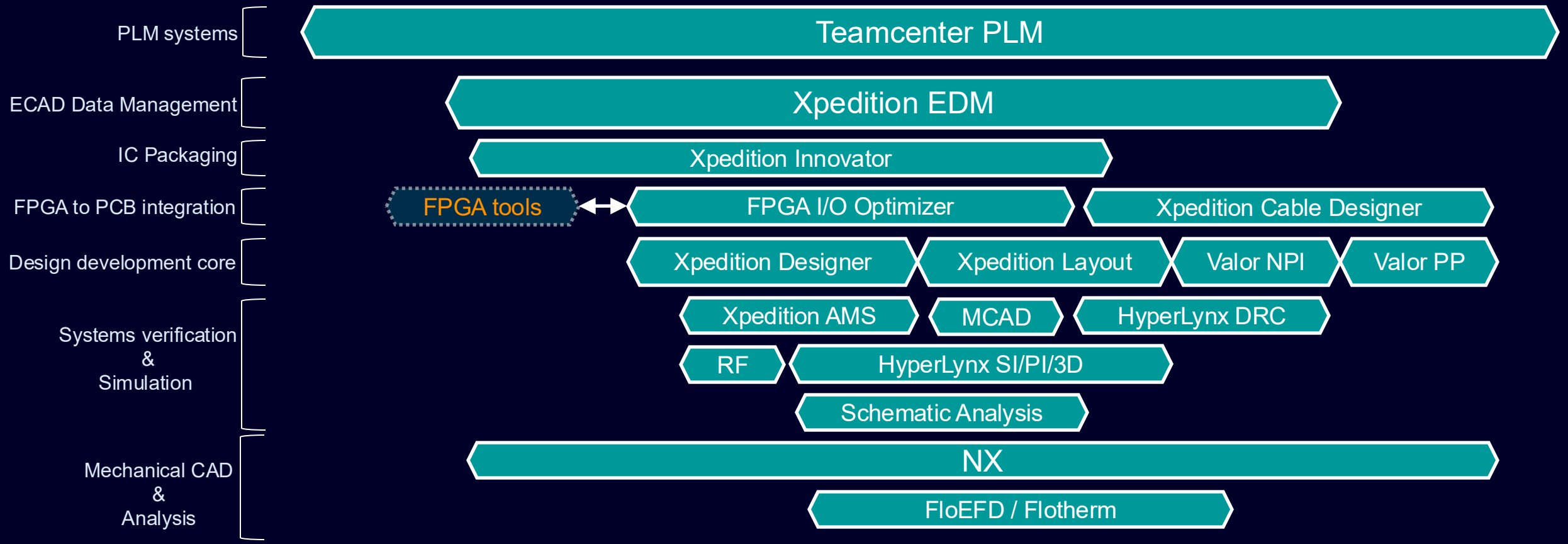
The Xpedition Digital Thread Ecosystem



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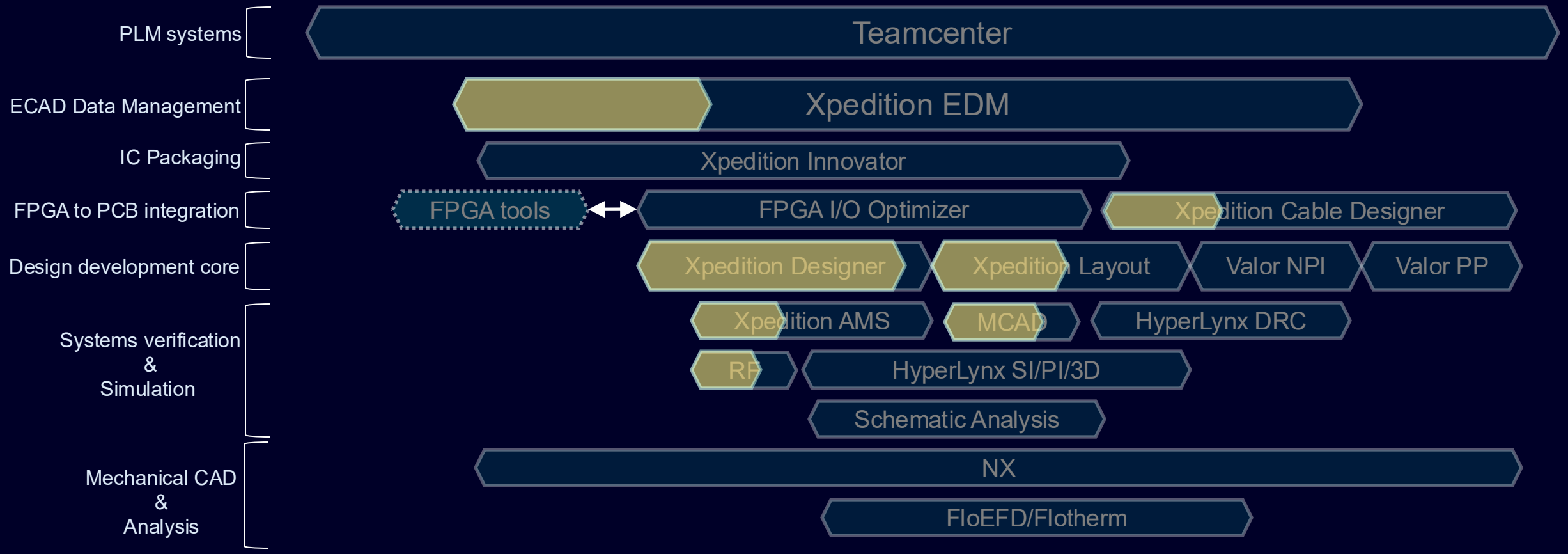
Siemens EDA vs Altium



Altium capabilities

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Integrations

- Teamcenter/EDM integration (7min34)
- ECAD/MCAD integration (3min37)
- Supply Frame integration (1min)
- HyperLynx Schematic Analysis integration (1min50)
- HyperLynx DRC integration (58s)
- HyperLynx PI / FloEFD integration (2min)
- DFM integration (53s)
- Xpedition MBE integration (8min)

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[PCB_SC100_L8.SoC_FPGA_Host.COVER]

Xpedition Designer

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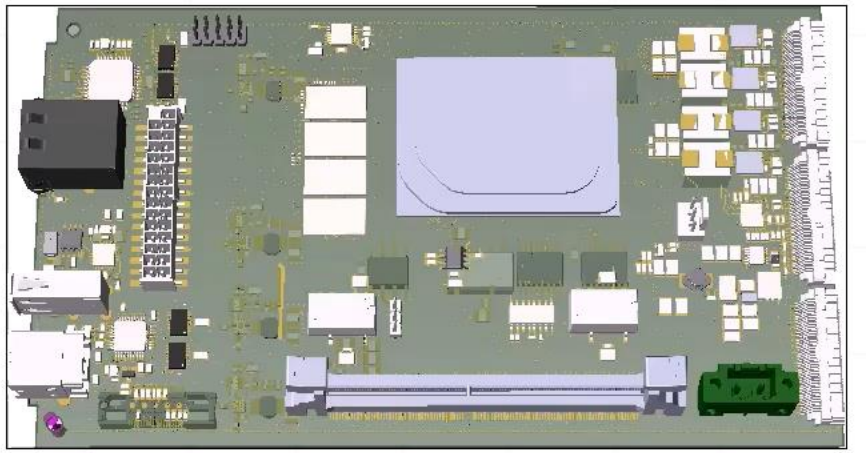
Navigator

Project

- PCB_SC100_L8
  - Boards
    - Board1
      - SoC_FPGA_Host
        - COVER
        - TOP_LEVEL
          - Symbols
            - DDR4
            - FPGA
            - Peripherals
              - 1
                - Symbols
                  - CLK_1
                  - DEBUG_1
                  - ETH_1
                    - 1
                  - FLASH_1
                  - Reset_1
                  - UART_1
                  - USB_PHY
                - Nets
            - PSU
          - Nets
        - CONN_UART
        - CONN_BACKPLANE
        - CONN_SODIMM
  - Blocks

SoC_FPGA_Hos... | Ethernet.1

Table of Contents	
1	COVER
2	TOP_LEVEL
3	DDR4 . 1
4	FPGA . 1
5	FPGA . BANK2_AB
6	FPGA . BANK2_CD
7	FPGA . BANK3_AB
8	FPGA . BANK3_CD
9	FPGA . BANK9
10	FPGA . BANK10
11	FPGA . CONFIG
12	FPGA . GND1
13	FPGA . GND2
14	FPGA . GND3
15	FPGA . JTAG_NOBANK
16	FPGA . POWER
17	FPGA . HPS
18	FPGA . DECAP
19	PSU . 1
20	PSU\PSU_0\675_1 . 1
21	PSU\PSU_1\0_1 . 1
22	PSU\PSU_1\0_1\P1\0_Phase1 . 1
23	PSU\PSU_1\0_1\P1\0_Phase2 . 1
24	PSU\PSU_1\0_1\P1\0_Phase3 . 1
25	PSU\PSU_1\0_1\P1\0_Phase4 . 1
26	PSU\PSU_1\2_1 . 1
27	PSU\PSU_1\8_1 . 1
28	PSU\PSU_2\5_1 . 1
29	PSU\PSU_3\3_1 . 1
30	PSU\PSU_5\0_1 . 1
31	Peripherals . 1
32	Peripherals\CLK_1 . 1
33	Peripherals\DEBUG_1 . 1
34	Peripherals\ETH_1 . 1
35	Peripherals\FLASH_1 . 1
36	Peripherals\Reset_1 . 1
37	Peripherals\UART_1 . 1
38	Peripherals\USB_PHY . 1
39	Peripherals\USB_PHY . 2
40	CONN_UART
41	CONN_BACKPLANE
42	CONN_SODIMM



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TITLE: System Controller - 8L

SIZE	DWG NO		REV
A3	EBSD_SYS_L8	SoC_FPGA_Host COVER	03
DRAWN BY	SHEET	of	
EBS TME	1	42	29/08/2023:23:02

Message Window | Variant Manager

Select | 0 objects selected | EBSD | Library: \\sedaedm\EDM_Share\CL\LIB_EBSD\LIB_EBSD.lmc

Datum Plane | Sketch | Extrude | Hole | More | Board | Component | Area | Drilled Hole | More | Read PCB | Publish PCB | More | Design Rule Manager | Design Rule Explorer | Validate PCA | Compare and Update PCA | More | Import ECAD Model | Import ECAD Panel | More | Board Properties | Thermal Solution | Structural Solution | Show ECAD Primary Pin | Show MCAD Primary Pin | PCB Variant | Automatic Area Creation | Multi-Height Area Creation | More

Construction | Modeling | Attributes | Xpedition | Validation | Valor | Simulation | Tools

Menu | No Selection Filter | Entire Assembly

PCB Design Navigator

Refresh

Board

Name	Zone Board Name
pcb_sc100-nf_start_-1_1	

Component

Ref. Des.	Package Name	Part Number
J2002	LSHM-150-01-L...	4101-1021
J4000	c-292336-1-b-3d	4101-1042
J4001	c-292304-1-b-3d	4101-1043
J4007	HFJ11-1G01ER	4101-1007
J4027	xd_mictor_smt_1	4101-1023
J4399	IPL1-115-02-F-...	4101-1089
M1	Heatsink	WV_HSF-55-24
U1	BGA	6251-0500

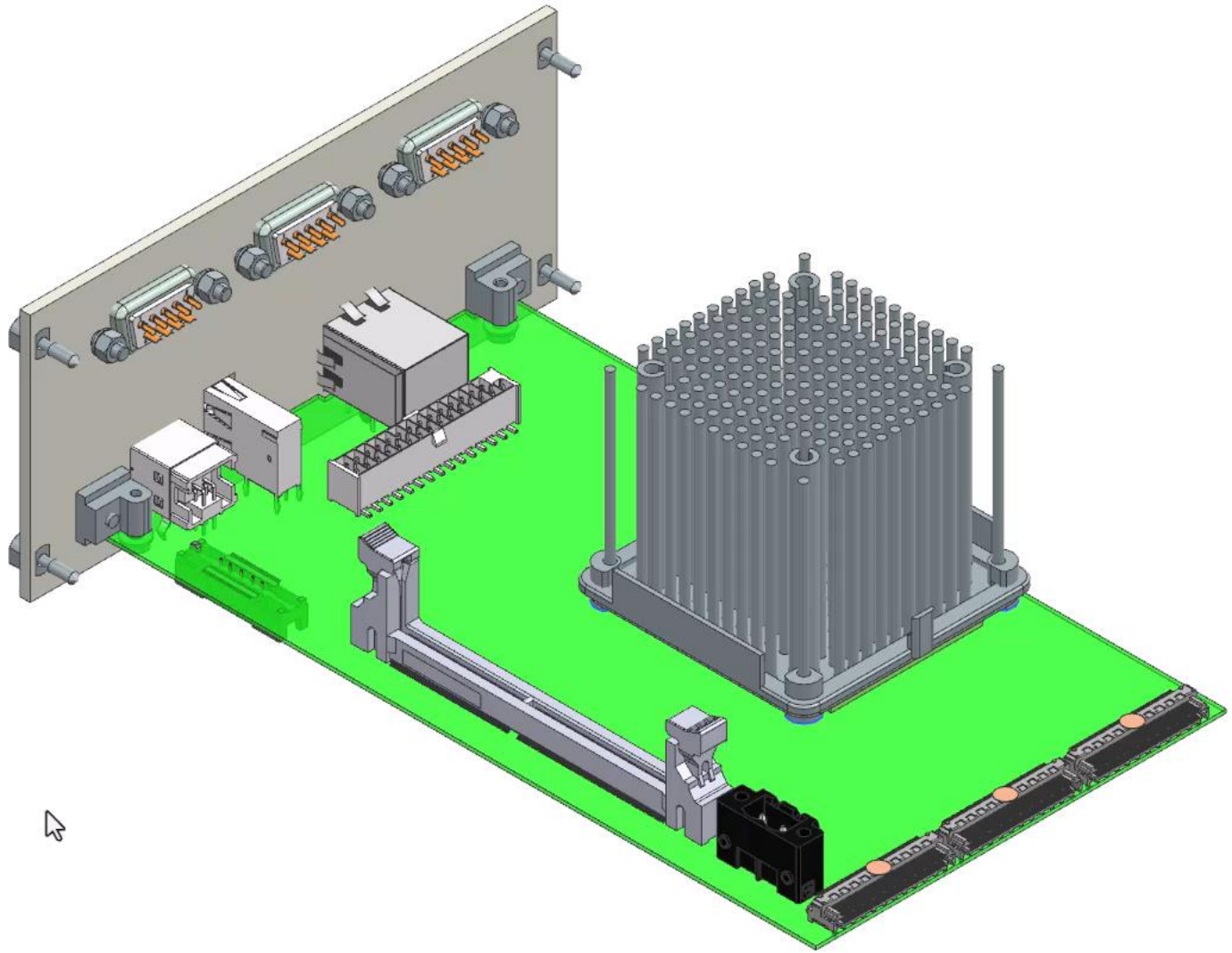
Area

Hole

Type	Associated Part	Owner	Pl
Mounting	Board	Unowned	No
Mounting	Board	Unowned	No

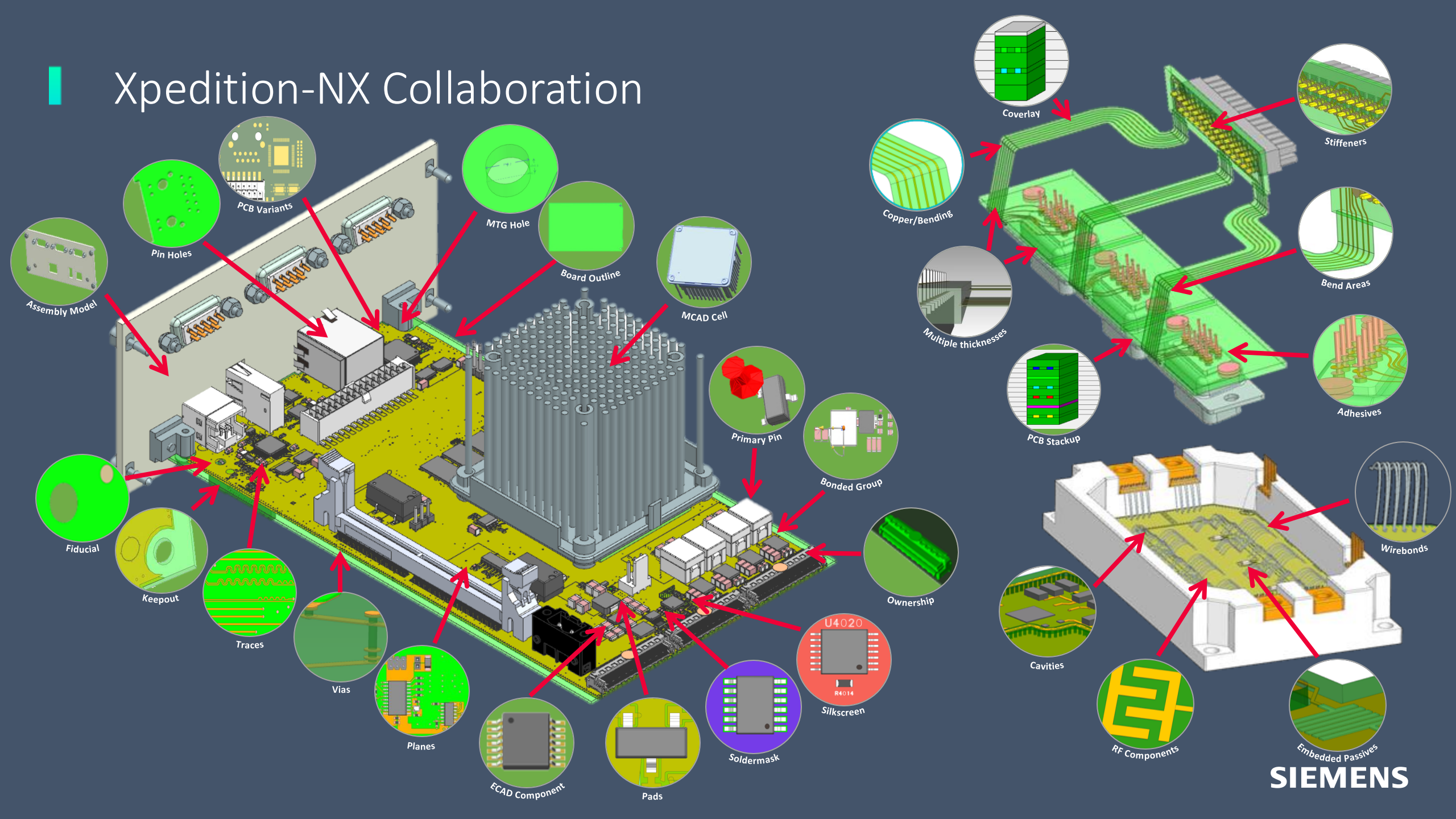
Net

PCB_SC100-NF_Start.prt



1 Notification

Xpedition-NX Collaboration



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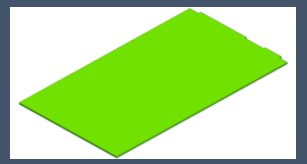
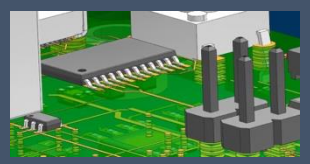
General Feature Capability

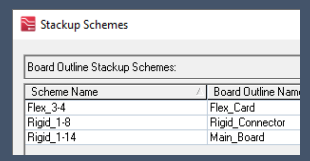
Saving modeling time with substrate support


PCB Outline

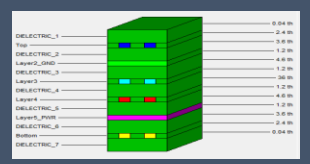

Cutout

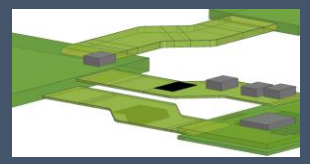

Cavities


PCB Stackup



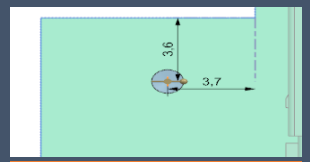
Stackup Schemes


Stackup Table

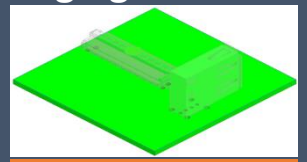

Flex Design

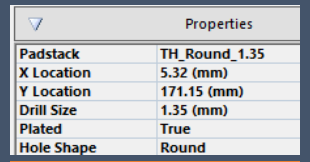

Stiffeners

Exchanging Hole and Padstack information

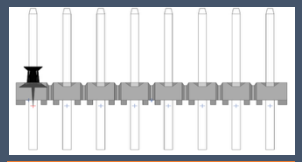


Holes

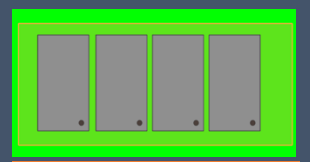

Comp MTG/Pin

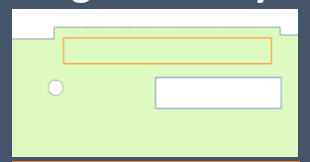


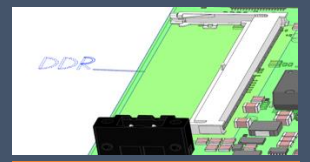
Hole Padstack


Primary Pin

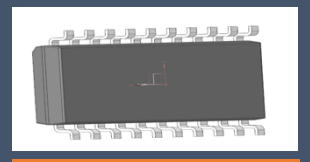
Defining Assembly Constraints and Notes


Room

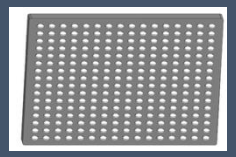

Keep out

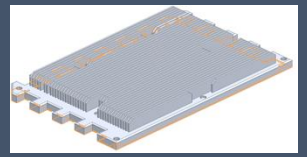


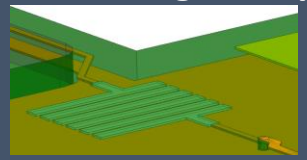
User Layer


Comp CSYS

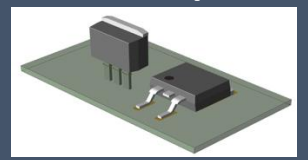
Enabling Enterprise collaboration with component collaboration

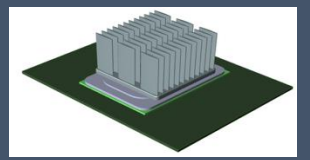

ECAD Comp

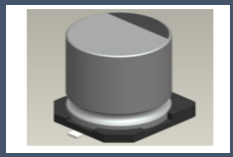

Mech Cell


Embedded Passives


RF

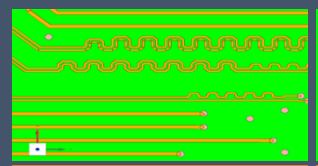

Alternate Cell

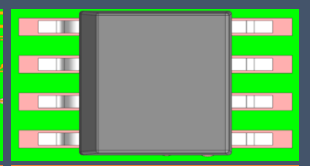

Nested Cell

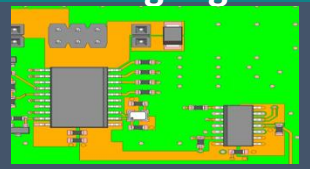

3D Exchange


Assembly Model

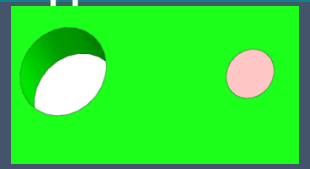
Increasing digital twin realism with copper in the mechanical assembly


Traces

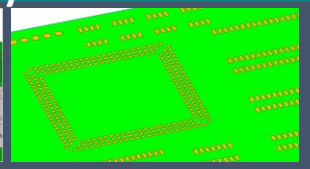

Pads

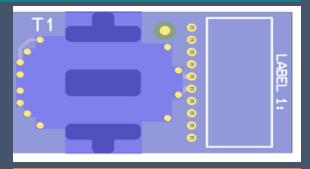

Copper Planes


Vias


Fiducials

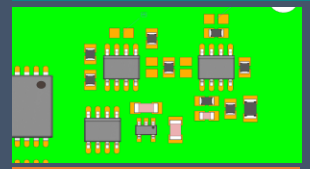

Wire Bonds

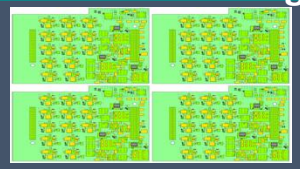

Soldermask

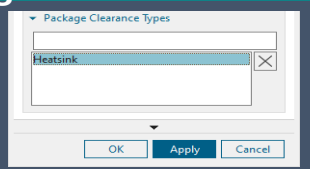


Silkscreen

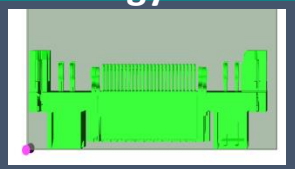
Delivering advanced PCB technology


PCB Variants


Panelization

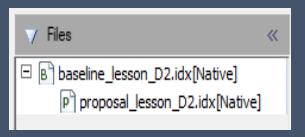


3D Clearances

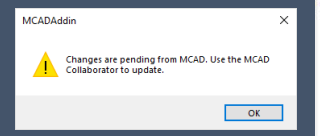

Ownership


Frozen Group

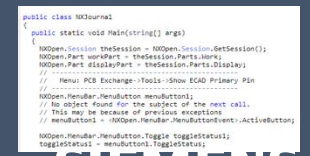
Managing the Collaboration Workflow



History



Notifications


Hooks

Power supply board for EB-SD

Design BOM Files Users History

Project Version

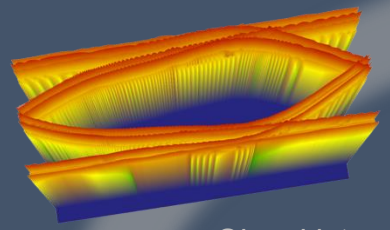
Version 2 | Created 2 days ago by Casey Silbernagel

Download Project

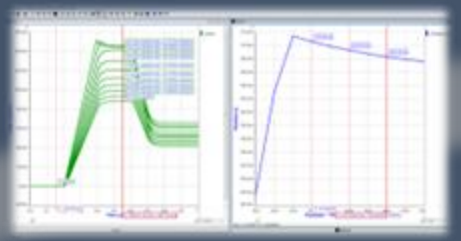
Name	Open as	Type	Modification Date	Last modified by
PCB_PS250		SCHEMATIC	2 days ago	Casey Silbernagel
PCB_PS250	2D 3D	LAYOUT	2 days ago	Casey Silbernagel

Increasing Product Complexity Demands Increased Verification

Leveraging a digital twin for early verification reduces system integration risk

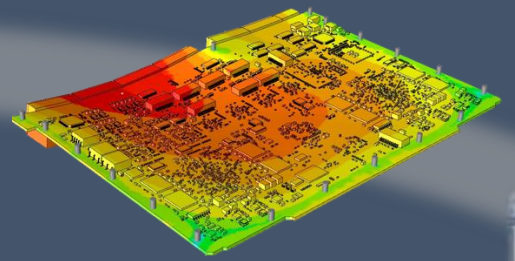


Signal integrity

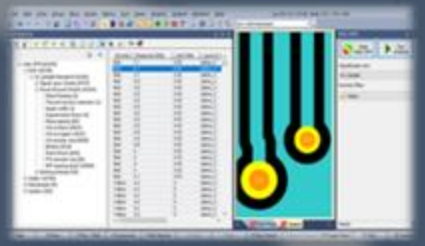


Analog/mixed signal

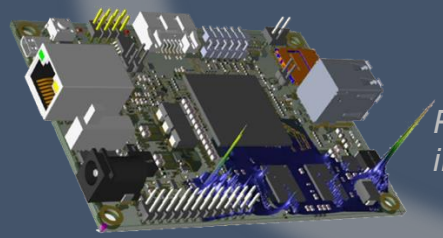
Schematic integrity



Vibration & stress

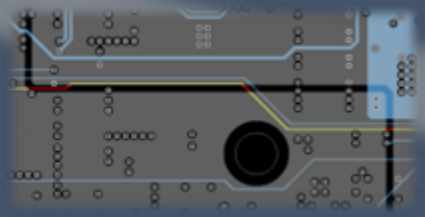


Manufacturability

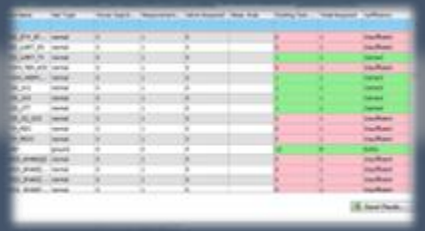


Power integrity

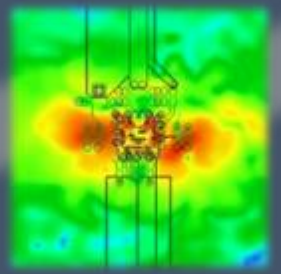
Electrical rule checking



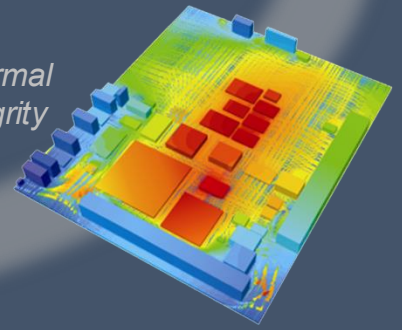
DFT



EMI



Thermal integrity

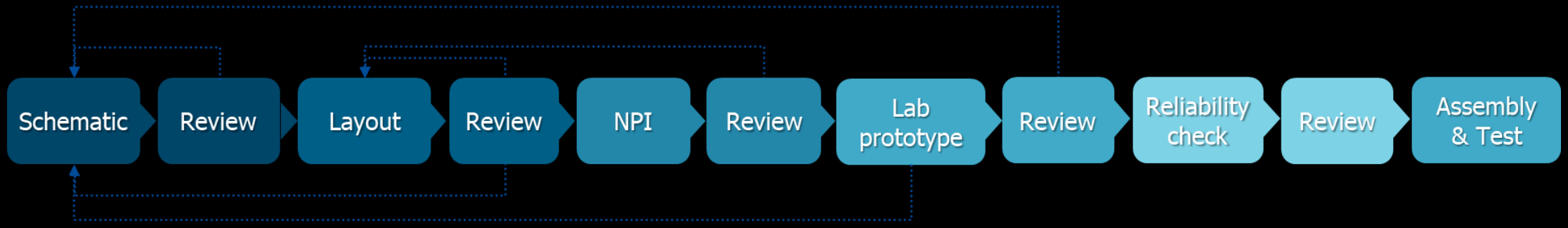


SIEMENS

The Siemens EDA Value: Revolutionize Electronic Design

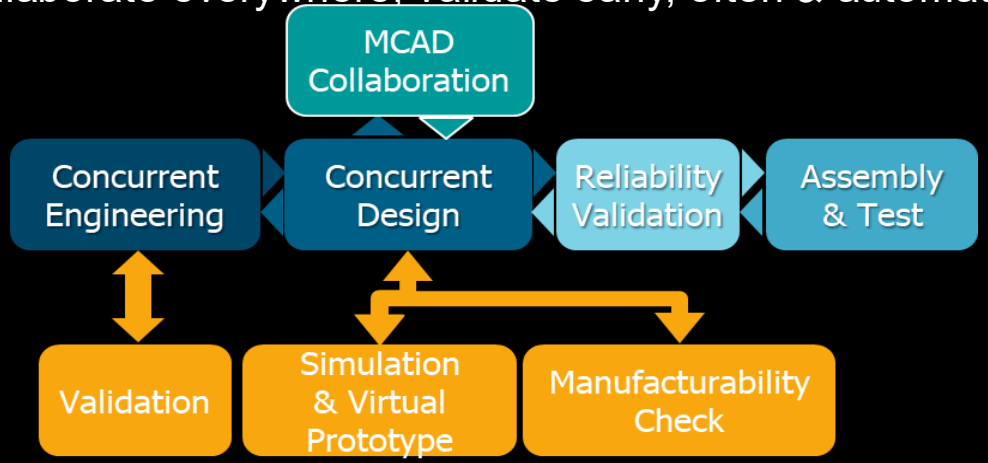
Conventional design process

Cycle time through manual inspection, incomplete coverage, and reliability issues adds re-spins



Siemens EDA shift-left approach

Collaborate everywhere, validate early, often & automatically - reducing cycle times and increasing quality



Shift Left Methodology

Cycle Time Reduction
Risk & Cost Reduction
Elimination of Design Spins

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Hyperlynx Schematic Analysis

HyperLynx Schematic Analysis

Search help...

SIEMENS

VPRJ

Project | BOM | Netlist | Voltage | Run | Results

MetaData

Project Name | Product Code

Company | Division | Project Owner | Project Owner Email

Boards

Board Name	BOM	Netlist	Designer Board Na	Variant	Designer Project File
new board	Import	Import			

Add | Delete

Connectors

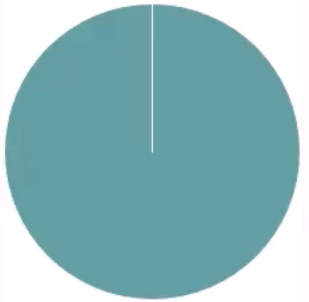
Connector Name	Left	Right

Import | Delete

Navigator

- new board
  - 0 Components
  - 0 Nets
  - 0 Voltages

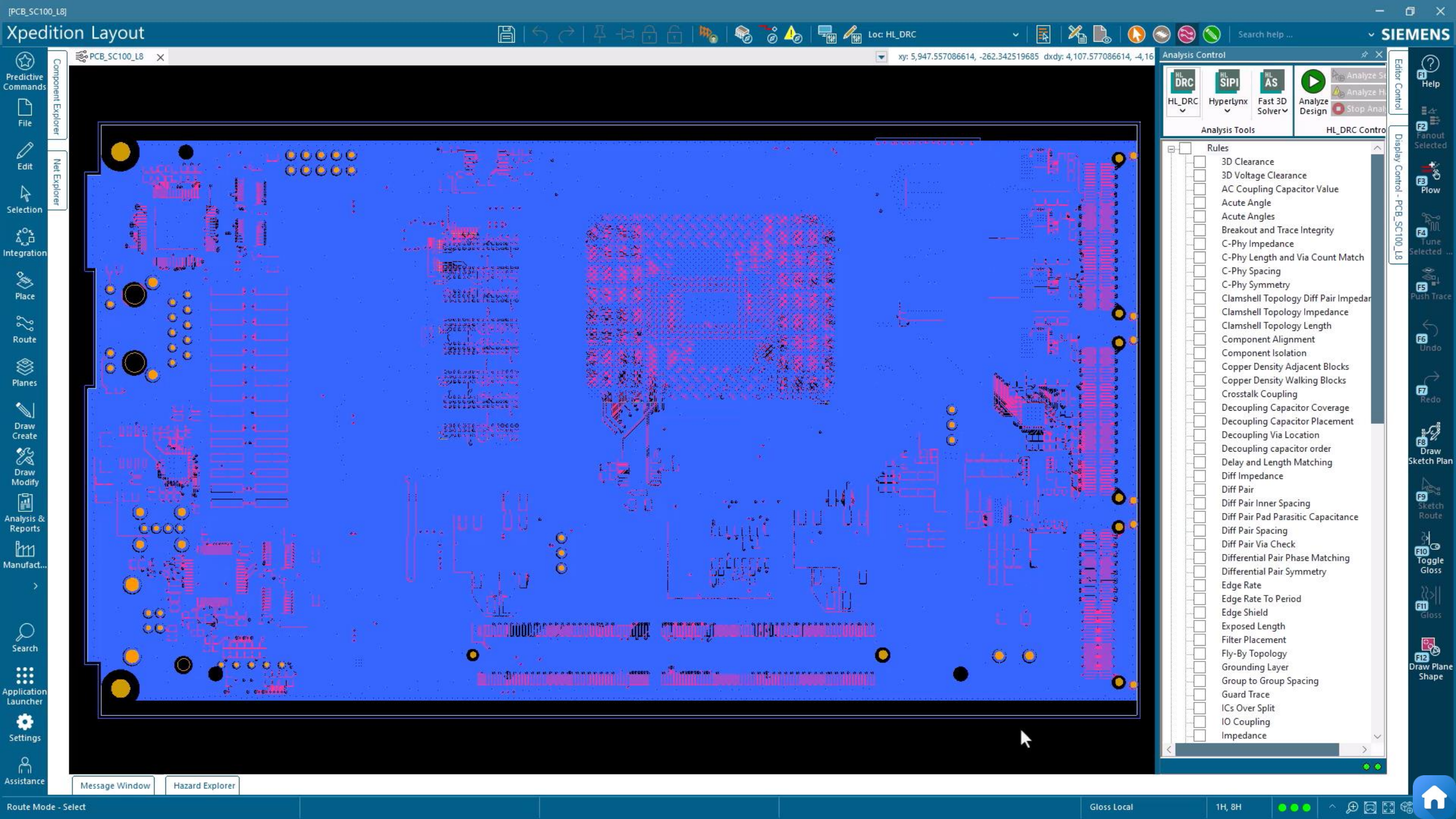
Project Statistics

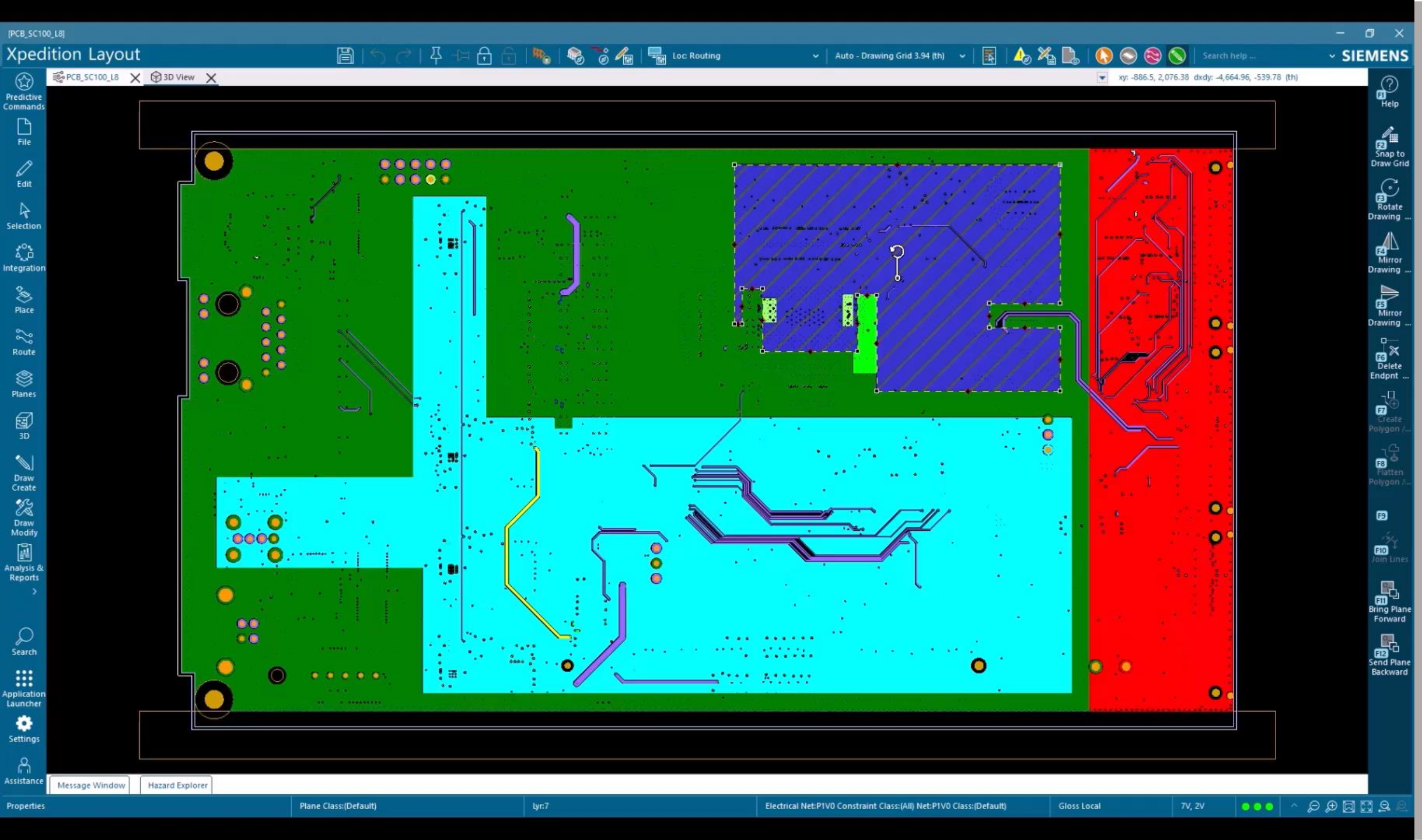


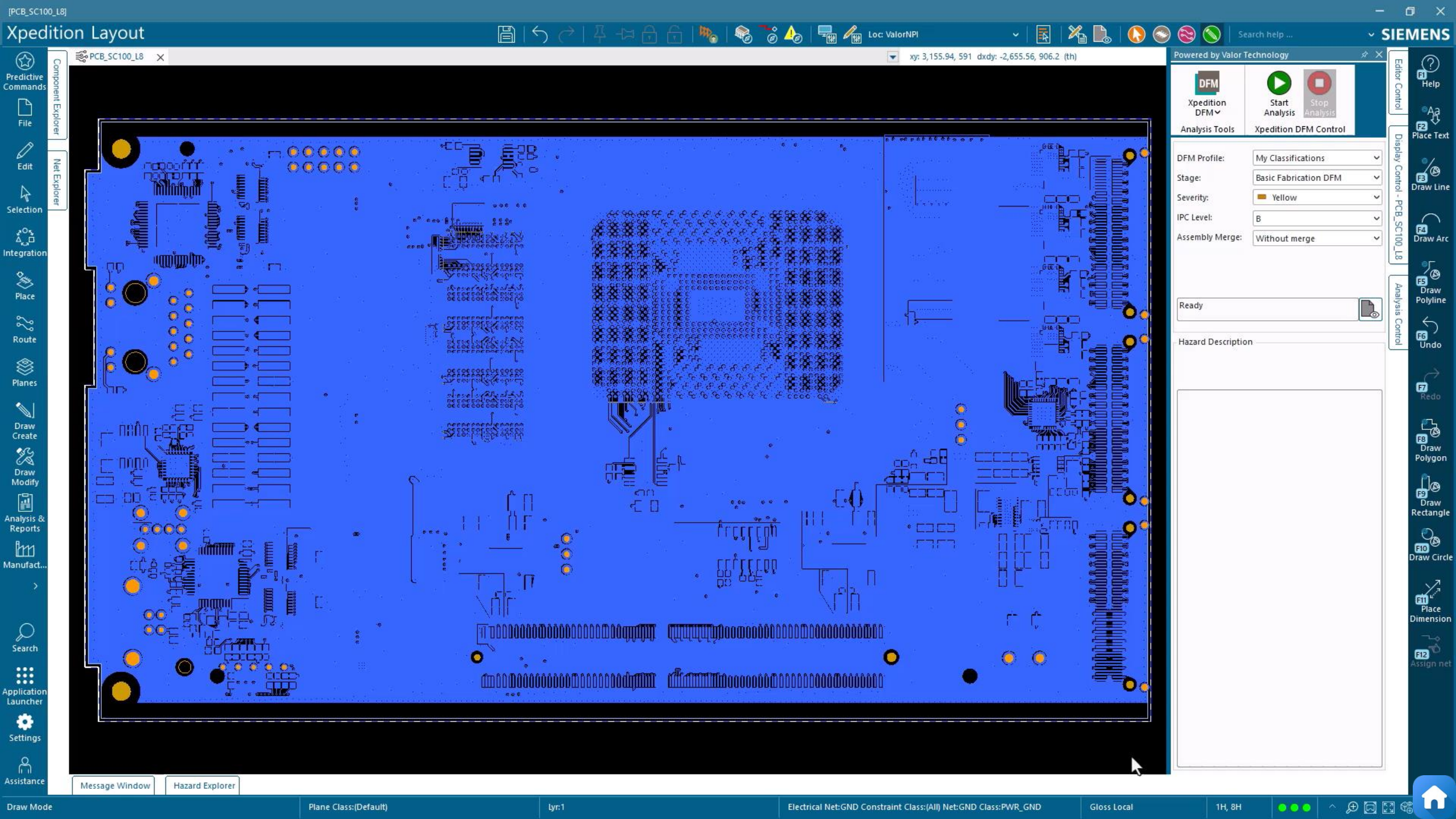
Critical	0
Defect	0
Warning	0
Nets Tested	0
Tests Performed	0
Results Stored	0

Output Log

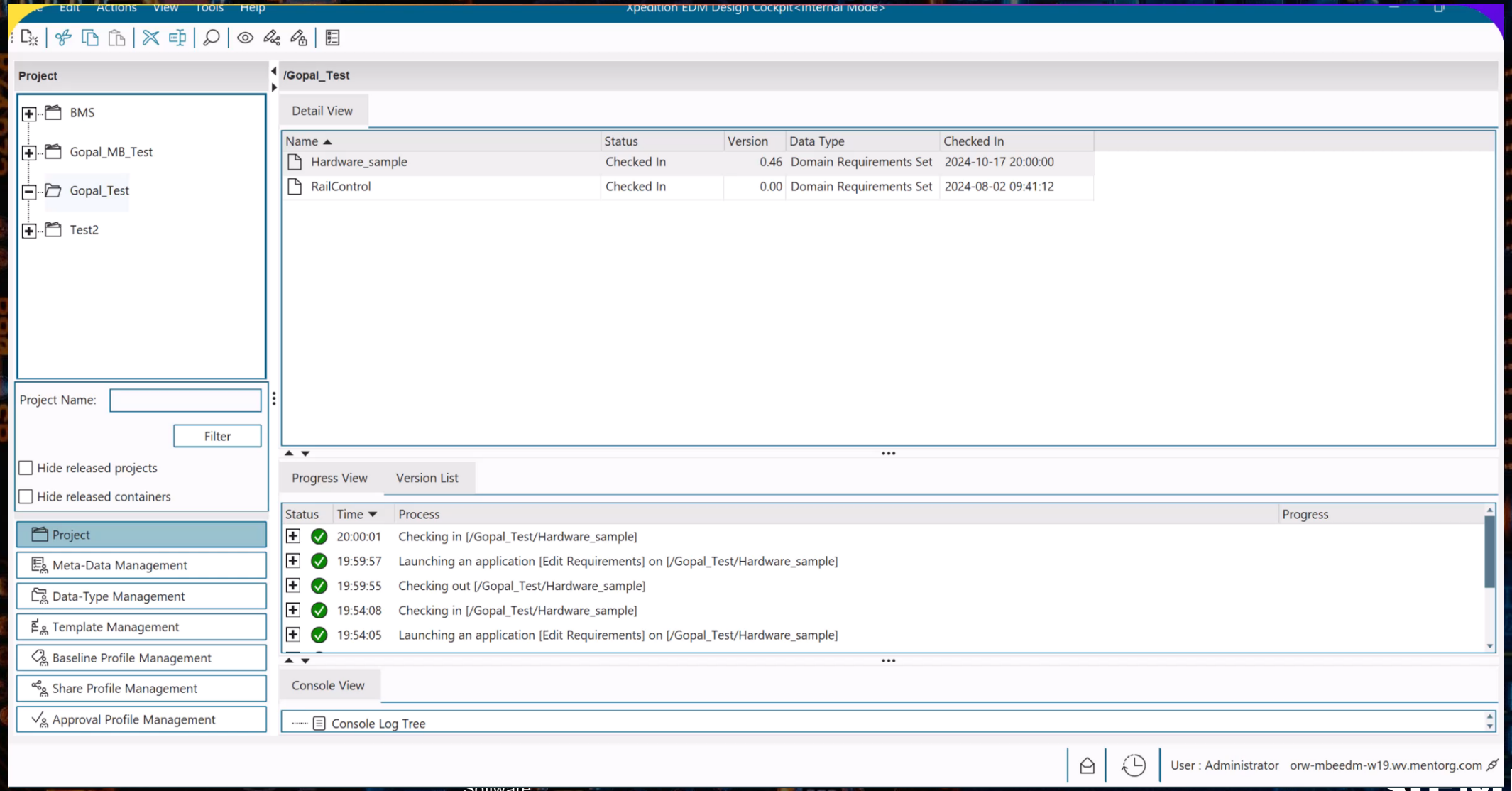
Closed current project.	14:4:47
Backed up project.	14:9:45
Backed up project.	14:14:45
Closed current project.	14:15:46


[PCB_SC100_L8]
Xpedition Layout
SIEMENS
Loc: HL_DRC
Search help ...
Predictive Commands
File
Edit
Selection
Integration
Place
Route
Planes
Draw Create
Draw Modify
Analysis & Reports
Manufact...
Search
Application Launcher
Settings
Assistance
Component Explorer
Net Explorer
PCB_SC100_L8
xy: 5,947.557086614, -262.342519685 dxdy: 4,107.577086614, -4,16
Analysis Control
HL_DRC
HyperLynx
Fast 3D Solver
Analyze Design
Analysis Tools
HL_DRC Contro
Editor Control
Display Control - PCB_SC100_L8
Rules
3D Clearance
3D Voltage Clearance
AC Coupling Capacitor Value
Acute Angle
Acute Angles
Breakout and Trace Integrity
C-Phy Impedance
C-Phy Length and Via Count Match
C-Phy Spacing
C-Phy Symmetry
Clamshell Topology Diff Pair Impedar
Clamshell Topology Impedance
Clamshell Topology Length
Component Alignment
Component Isolation
Copper Density Adjacent Blocks
Copper Density Walking Blocks
Crosstalk Coupling
Decoupling Capacitor Coverage
Decoupling Capacitor Placement
Decoupling Via Location
Decoupling capacitor order
Delay and Length Matching
Diff Impedance
Diff Pair
Diff Pair Inner Spacing
Diff Pair Pad Parasitic Capacitance
Diff Pair Spacing
Diff Pair Via Check
Differential Pair Phase Matching
Differential Pair Symmetry
Edge Rate
Edge Rate To Period
Edge Shield
Exposed Length
Filter Placement
Fly-By Topology
Grounding Layer
Group to Group Spacing
Guard Trace
ICs Over Split
IO Coupling
Impedance
Help
Fanout Selected
Plow
Tune Selected ...
Push Trace
Undo
Redo
Draw Sketch Plan
Sketch Route
Toggle Gloss
Gloss
Draw Plane Shape
Message Window
Hazard Explorer
Route Mode - Select
Gloss Local
1H, 8H


[PCB_SC100_L8]
Xpedition Layout
Loc Routing
Auto - Drawing Grid 3.94 (th)
Search help ...
SIEMENS
PCB_SC100_L8
3D View
xy: -886.5, 2,076.38 dxdy: -4,664.96, -539.78 (th)
Predictive Commands
File
Edit
Selection
Integration
Place
Route
Planes
3D
Draw Create
Draw Modify
Analysis & Reports
Search
Application Launcher
Settings
Assistance
Help
Snap to Draw Grid
Rotate Drawing ...
Mirror Drawing ...
Mirror Drawing ...
Delete Endpnt ...
Create Polygon /...
Flatten Polygon /...
Join Lines
Bring Plane Forward
Send Plane Backward
Message Window
Hazard Explorer
Properties
Plane Class:(Default)
Lyr:7
Electrical Net:P1V0 Constraint Class:(All) Net:P1V0 Class:(Default)
Gloss Local
7V, 2V


[PCB_SC100_L8]
Xpedition Layout
SIEMENS
Loc: ValorNPI
Search help ...
Predictive Commands
File
Edit
Selection
Integration
Place
Route
Planes
Draw Create
Draw Modify
Analysis & Reports
Manufact...
Search
Application Launcher
Settings
Assistance
Component Explorer
Net Explorer
PCB_SC100_L8
xy: 3,155.94, 591 dxdy: -2,655.56, 906.2 (th)
Powered by Valor Technology
Xpedition DFM
Start Analysis
Stop Analysis
Analysis Tools
Xpedition DFM Control
DFM Profile:
My Classifications
Stage:
Basic Fabrication DFM
Severity:
Yellow
IPC Level:
B
Assembly Merge:
Without merge
Ready
Hazard Description
Editor Control
Display Control - PCB_SC100_L8
Analysis Control
F1 Help
F2 Place Text
F3 Draw Line
F4 Draw Arc
F5 Draw Polyline
F6 Undo
F7 Redo
F8 Draw Polygon
F9 Draw Rectangle
F10 Draw Circle
F11 Place Dimension
F12 Assign net
Message Window
Hazard Explorer
Draw Mode
Plane Class:(Default)
Lyr:1
Electrical Net:GND Constraint Class:(All) Net:GND Class:PWR_GND
Gloss Local
1H, 8H

Xpedition MBE integration



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Digital Transformation Key Areas

Library Management

Centrally manage component libraries, ensuring consistency, version control, and compliance with industry standards like IPC. Ability to access rich metadata, track obsolescence, and integrate with supply chain data for procurement decisions.

ECAD Design Analysis

Provide system's simulation capabilities, including signal and power integrity analysis, thermal performance, and electromagnetic compatibility. Integrated analysis tools help engineers validate designs and make informed decisions early in the design cycle.

ECAD Collaboration

Real-time collaboration features, such as concurrent editing, live commenting, and structured design reviews. Streamline communication between electrical, mechanical, and other engineering teams through role-based access control and workflow management

ECAD Design Flow

Provide a complete PCB design process, from schematic capture and component placement to routing and manufacturability checks. Streamline the workflow and reduce design errors through design rules, constraints, and templates

Integrations

Seamless data exchange between ECAD, MCAD, PLM, and supply chain systems. Integrations enable BOM management, bidirectional updates with mechanical design tools, and automated workflows for design approvals and releases.

Infrastructure

Authentication, role-based access, and encryption features ensure data security. System administration capabilities, including audit logs, high availability, cloud/on-prem deployment options, and compliance with enterprise IT policies.

Support

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Thank You!

- **Olivier ARNAUD – olivier.arnaud@siemens.com**
- **Siemens EDA**
- **Applications Engineer Consultant - ECC**

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